



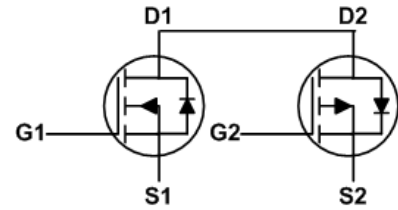
- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

Description

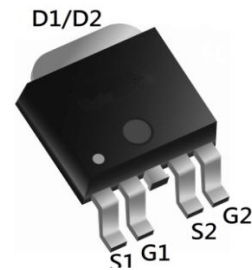
The WLU4012 is a high performance complementary N-ch and P-ch MOSFETs with high cell density, which provide excellent R_{DS(on)} and gate charge for most of the synchronous buck converter applications. The WLU4012 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

Product Summary

BVDSS	R _{DS(on)}	I _D
40V	17mΩ	25A
-40V	32mΩ	-25A



TO252-4 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
V _{DS}	Drain-Source Voltage	40	-40	V
V _{GS}	Gate-Source Voltage	±20	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	25	-25	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ¹	18	-16	A
I _{DM}	Pulsed Drain Current ²	46	-40	A
EAS	Single Pulse Avalanche Energy ³	28	66	mJ
I _{AS}	Avalanche Current	17.8	-27.2	A
P _D @T _C =25°C	Total Power Dissipation ⁴	25	31.3	W
T _{STG}	Storage Temperature Range	-55 to 150	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	62	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	5	°C/W



N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=40V, V_{GS}=0V$	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.5	2.5	V
$R_{DS(on)}$	Static Drain-Source on-Resistance <small>note3</small>	$V_{GS}=10V, I_D=8A$	-	17	22	m Ω
		$V_{GS}=4.5V, I_D=5A$	-	25	35	m Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=20V, V_{GS}=0V,$ $f=1.0MHz$	-	633	-	pF
C_{oss}	Output Capacitance		-	67	-	pF
C_{riss}	Reverse Transfer Capacitance		-	58	-	pF
Q_g	Total Gate Charge	$V_{DS}=20V, I_D=8A,$ $V_{GS}=10V$	-	12	-	nC
Q_{gs}	Gate-Source Charge		-	3.2	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	3.1	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=20V, R_L=2.5\Omega$ $V_{GS}=10V, R_{REN}=3\Omega$	-	4	-	ns
t_r	Turn-on Rise Time		-	3	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	15	-	ns
t_f	Turn-off Fall Time		-	2	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	20	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	32	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0V, I_S=8A$	-	-	1.2	V

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition : $T_J=25^\circ\text{C}, V_{DD}=20V, V_G=10V, L=0.5mH, R_g=25\Omega, I_{AS}=7.2A$

$T_J=25^\circ\text{C}, V_{DD}=-20V, V_G=-10V, L=0.5mH, R_g=25\Omega, I_{AS}=-8.4A$

3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$



P-Channel Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-40	---	---	V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.012	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-8A	---	35	45	mΩ
		V _{GS} =-4.5V, I _D =-4A	---	47	70	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-1.0	-1.6	-2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	4.32	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-32V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =-32V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-8A	---	12.6	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	13	16	Ω
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-20V, V _{GS} =-4.5V, I _D =-12A	---	9	---	nC
Q _{gs}	Gate-Source Charge		---	2.54	---	
Q _{gd}	Gate-Drain Charge		---	3.1	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =-15V, V _{GS} =-10V, R _G =3.3Ω, I _D =-1A	---	19.2	---	ns
T _r	Rise Time		---	12.8	---	
T _{d(off)}	Turn-Off Delay Time		---	48.6	---	
T _f	Fall Time		---	4.6	---	
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	1004	---	pF
C _{oss}	Output Capacitance		---	108	---	
C _{rss}	Reverse Transfer Capacitance		---	80	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	-20	A
I _{SM}	Pulsed Source Current ^{2,5}		---	---	-40	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The EAS data shows Max. rating . The test condition is V_{DD}=-25V,V_{GS}=-10V,L=0.1mH,I_{AS}=-27.2A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



Typical Performance Characteristics-N

Figure 1: Output Characteristics

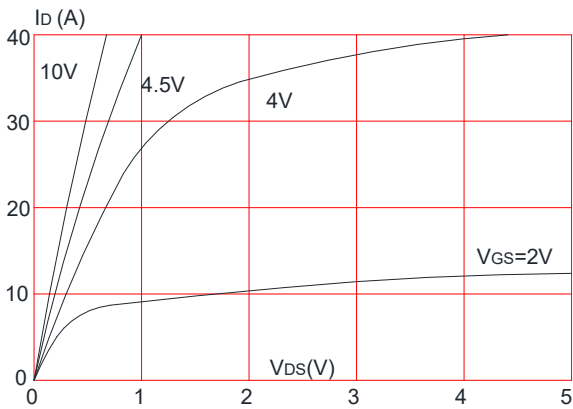


Figure 2: Typical Transfer Characteristics

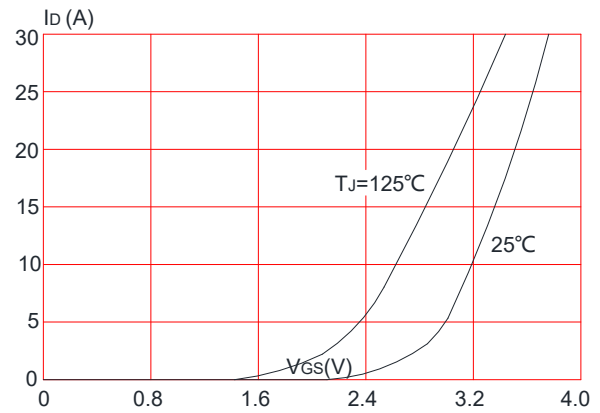


Figure 3: On-resistance vs. Drain Current

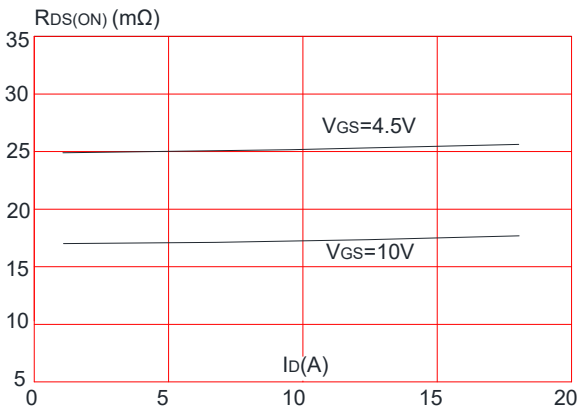


Figure 4: Body Diode Characteristics

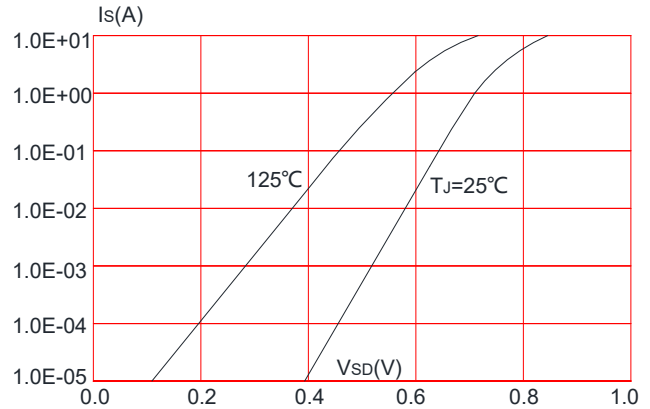


Figure 5: Gate Charge Characteristics

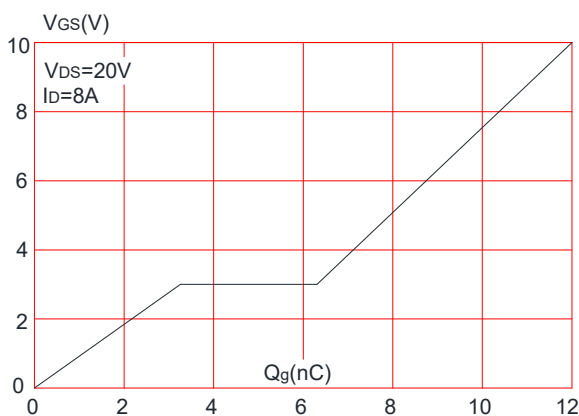


Figure 6: Capacitance Characteristics

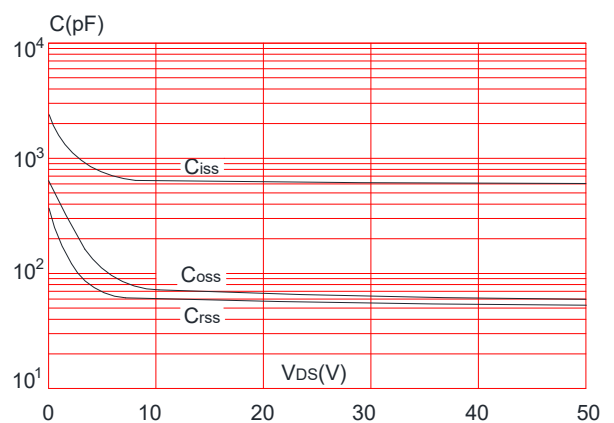




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

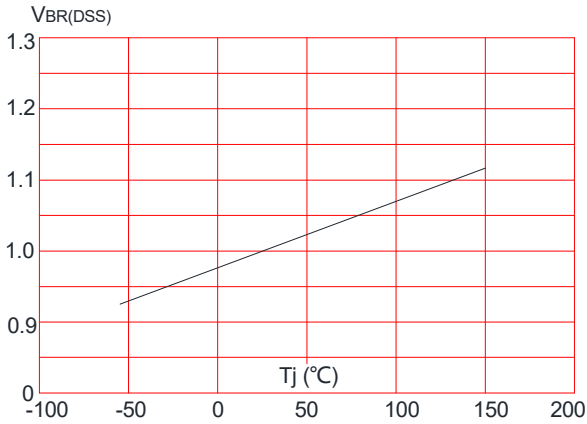


Figure 8: Normalized on Resistance vs. Junction Temperature

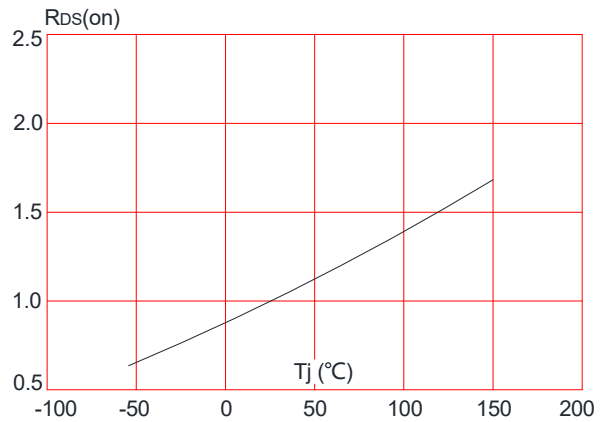


Figure 9: Maximum Safe Operating Area

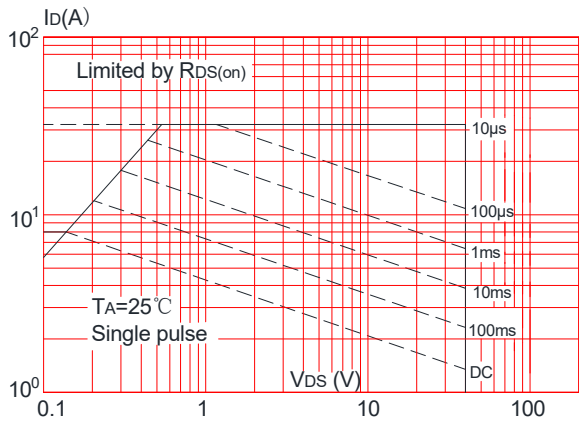


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

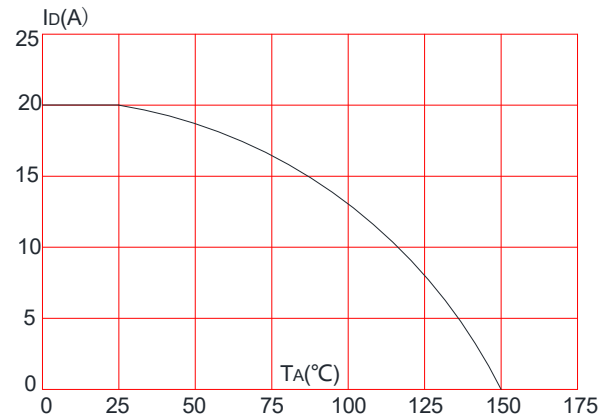
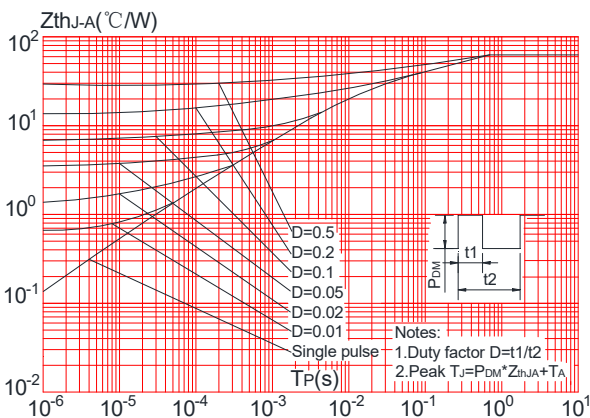


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient





P-Channel Typical Characteristics

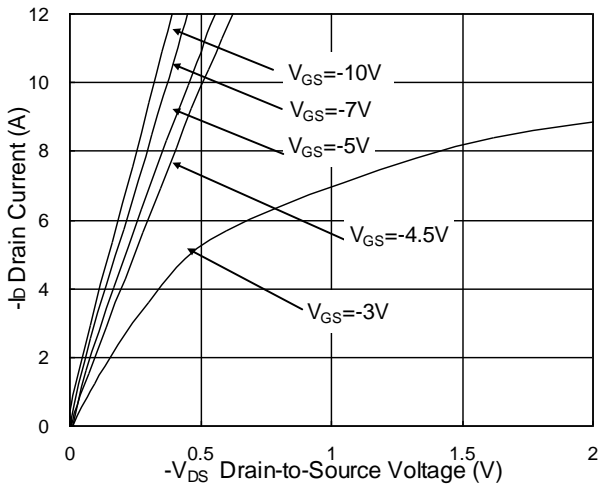


Fig.1 Typical Output Characteristics

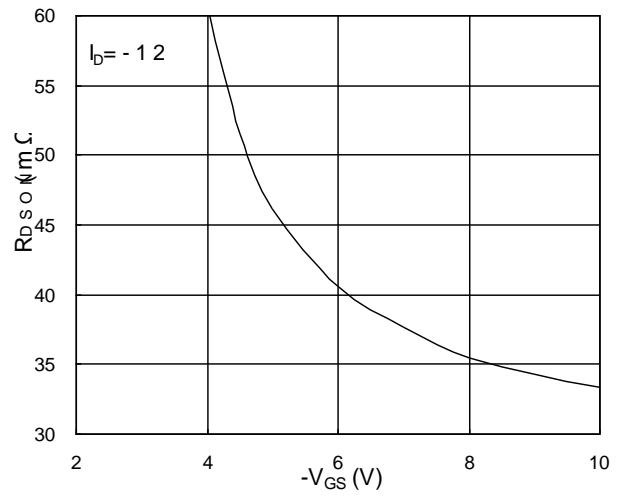


Fig.2 On-Resistance v.s Gate-Source

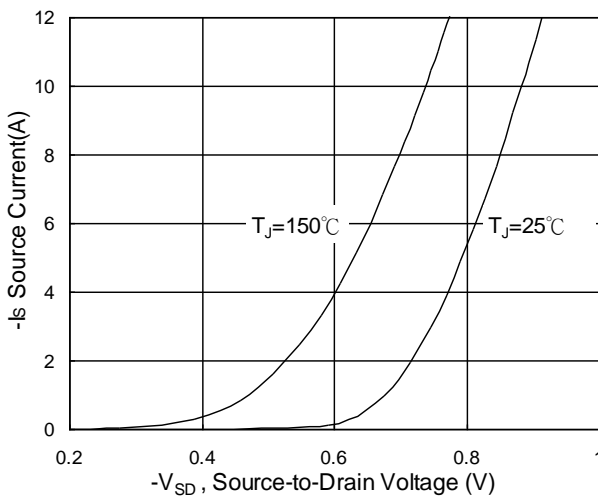


Fig.3 Forward Characteristics of Reverse

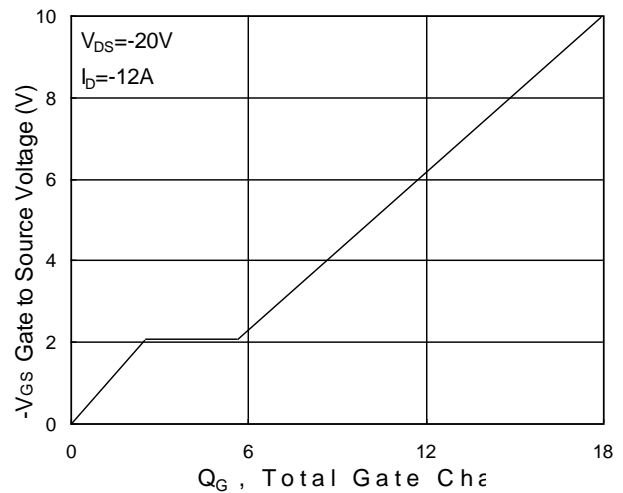


Fig.4 Gate-Charge Characteristics

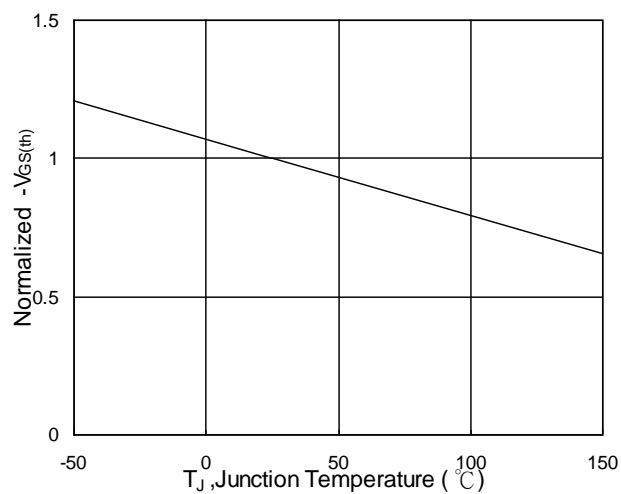


Fig.5 Normalized VGS(th) v.s TJ

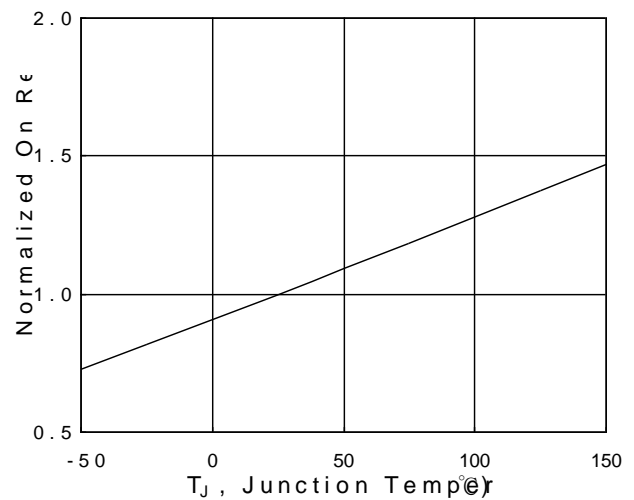


Fig.6 Normalized RDS(on) v.s TJ

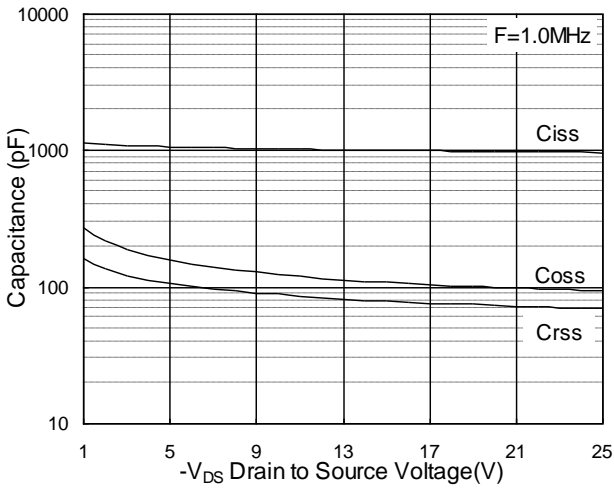


Fig.7 Capacitance

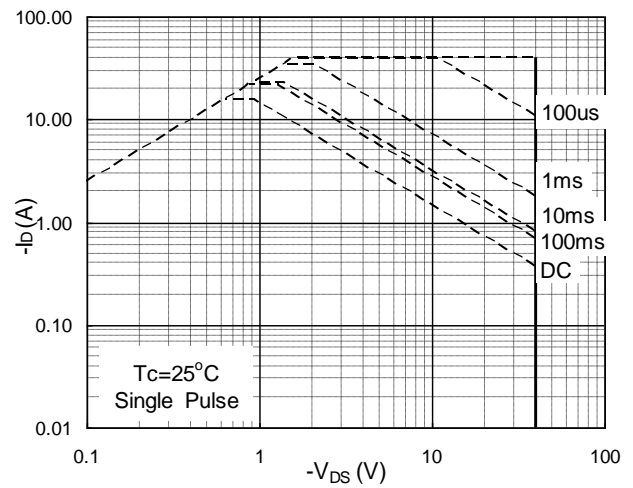


Fig.8 Safe Operating Area

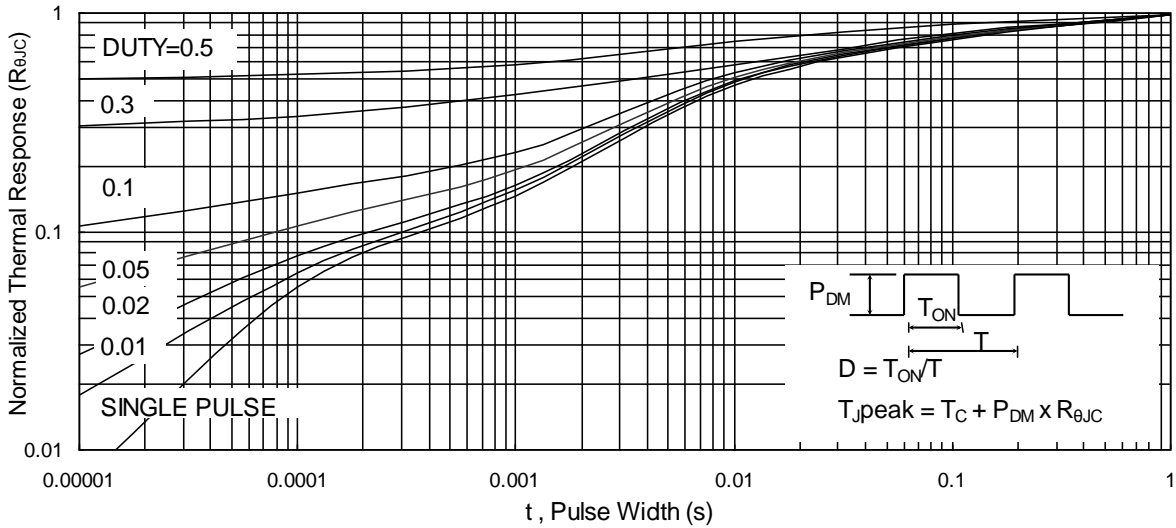


Fig.9 Normalized Maximum Transient Thermal Impedance

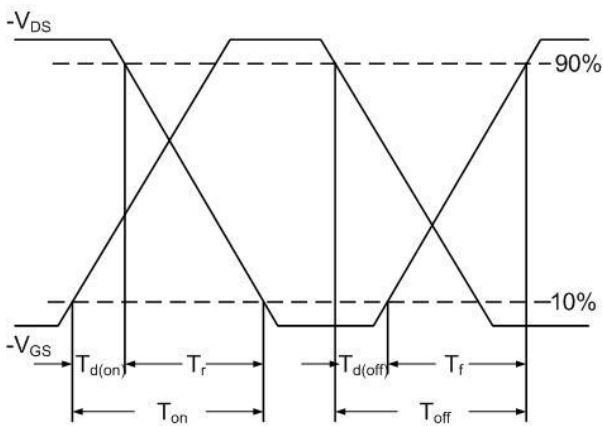


Fig.10 Switching Time Waveform

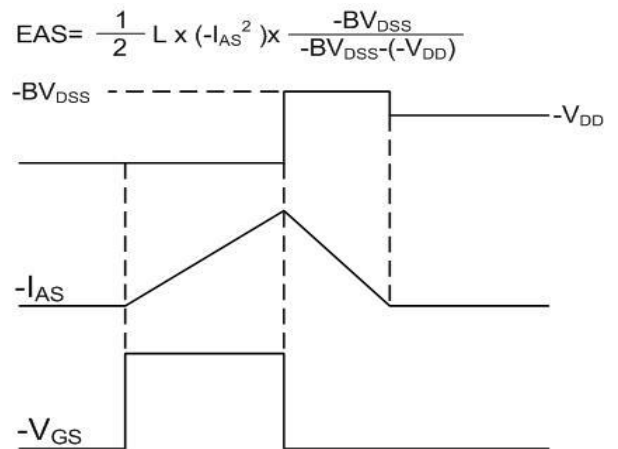
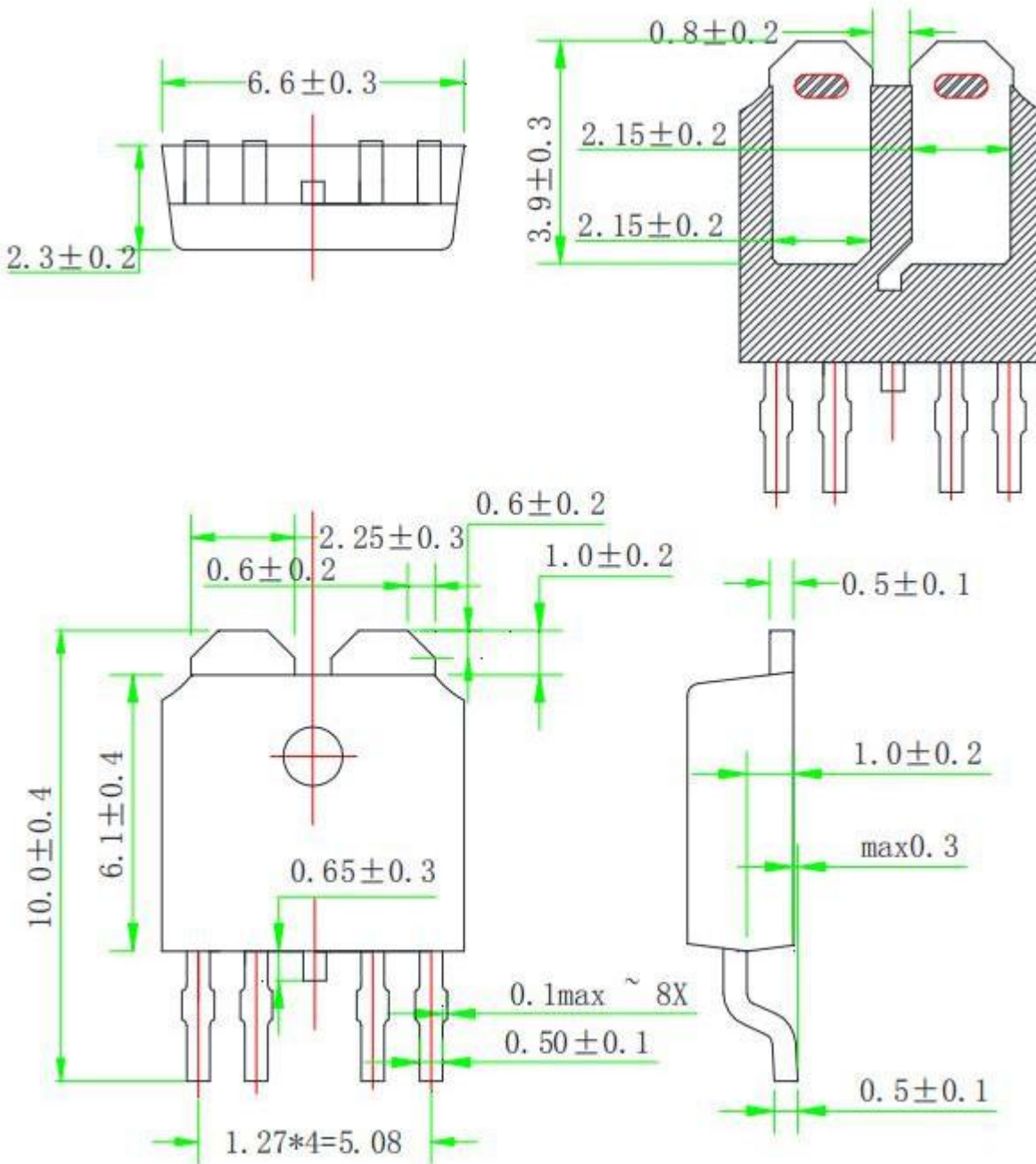


Fig.11 Unclamped Inductive Waveform

$$EAS = \frac{1}{2} L \times (-I_{AS}^2) \times \frac{-BV_{DSS}}{-BV_{DSS} - (-V_{DD})}$$



TO-252 Package outline





Disclaimer

Brunei has made reasonable commercial efforts to ensure that the information given in this datasheet is correct. However, it must clearly be understood that such information is for guidance only and does not constitute any representation or form part of any offer or contract.

For documents and material available from this datasheet, Brunei does not warrant or assume any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, product, technology or process disclosed hereunder.

Brunei reserves the rights to at its own discretion to make any changes or improvements to this datasheet. Unless said datasheet is incorporated into the formal contract, any customer should not rely on the information as any specification or product parameters duly committed by Brunei. Customers are hereby advised to verify that the information contained herein is current and complete before the entering of any contract or acknowledgement of any purchase order. Accordingly, all products specified hereunder shall be sold subject to Brunei's terms and conditions supplied at the time of order acknowledgement. Except where agreed upon by contractual agreement, testing of all parameters of each product is not necessarily performed.

Brunei does not warrant or convey any license either expressed or implied under its patent rights, nor the rights of others. Reproduction of information contained herein shall be only permissible if such reproduction is without any modification or alteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. Brunei is not responsible or liable for such altered documentation.

Resale of Brunei's products with statements different from or beyond the parameters stated by Brunei for that product or service voids all express or implied warranties for the associated Brunei's product or service and is unfair and deceptive business practice. Brunei is not responsible or liable for any such statements.

Brunei's products are not authorized for use as critical components in life support devices or systems without the express written approval of Brunei. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.