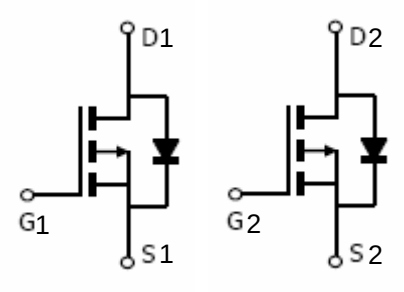
WLQ07P03

Dual P-Channel Enhancement Mode Field Effect Transistor

Description

The WLQ07P03 is uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in load switch and battery protection applications.

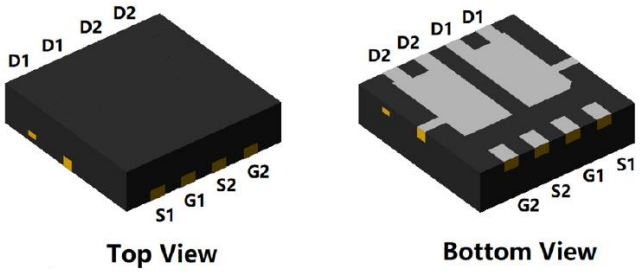


Application

- Load switch
- battery protection

General Features

- V_{DS} =-30V,I_D =-7A
  $R_{DS(ON)}$ = 27mΩ @ V_{GS}=-10V
  $R_{DS(ON)}$ = 38mΩ @ V_{GS}=-4.5V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current



DFN3.3X3.3-8L(Dual)

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-7	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	-4.5	A
Pulsed Drain Current	I_{DM}	-30	A
Maximum Power Dissipation	P_D	3.1	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient(Note 2)	$R_{\theta JA}$	40	℃/W

Electrical Characteristics (T_A=25℃unless otherwise noted)

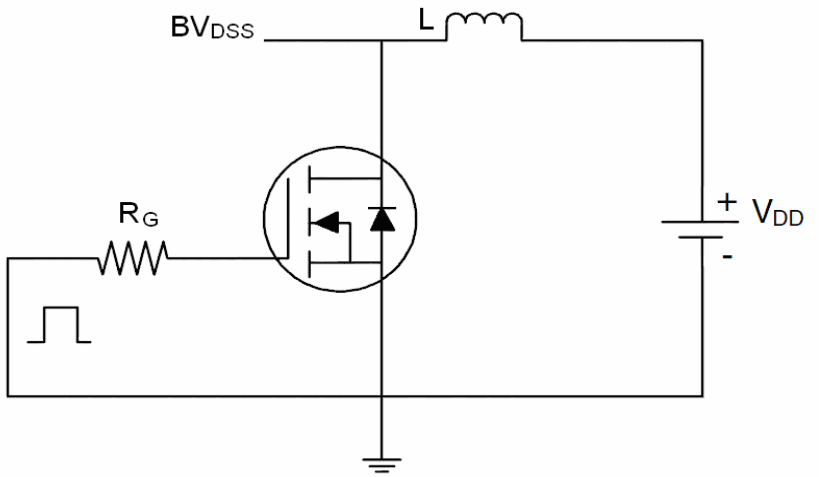
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-30	-34	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1.0	-1.5	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-7A	-	27	35	mΩ
		V_{GS}=-4.5V, I_D=-4A	-	38	54	
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-7A	-	15	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=-30V,V_{GS}=0V, F=1.0MHz	-	942	-	PF
Output Capacitance	C_{oss}		-	165	-	PF
Reverse Transfer Capacitance	C_{rss}		-	137	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-30V,I_D=-4A V_{GS}=-20V, R_{GEN}=3.3 Ω	-	16.4	-	nS
Turn-on Rise Time	t_r		-	20.2	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	55	-	nS
Turn-Off Fall Time	t_f		-	10	-	nS
Total Gate Charge	Q_g	V_{DS}=-30V,I_D=-7A, V_{GS}=-4.5	-	9.5	-	nC
Gate-Source Charge	Q_{gs}		-	2	-	nC
Gate-Drain Charge	Q_{gd}		-	3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-7A	-	-0.75	-1.2	V
Diode Forward Current (Note 2)	I_S		-	-	-6.5	A

Notes:

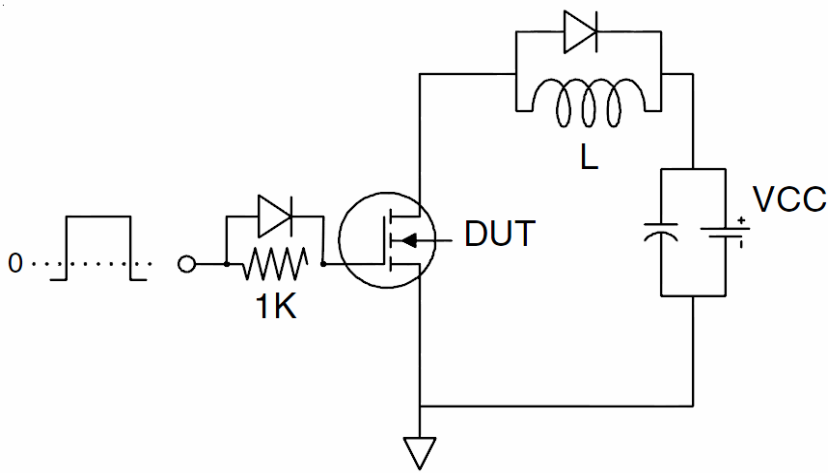
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Test Circuit

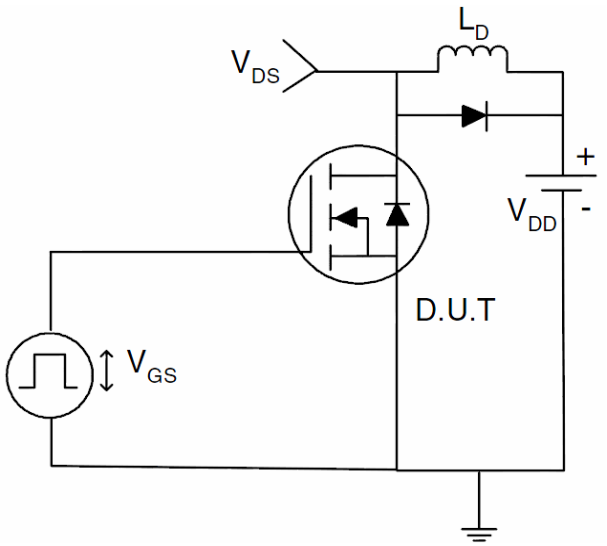
1)E_{AS} test Circuit



2) Gate charge test Circuit



3) witch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

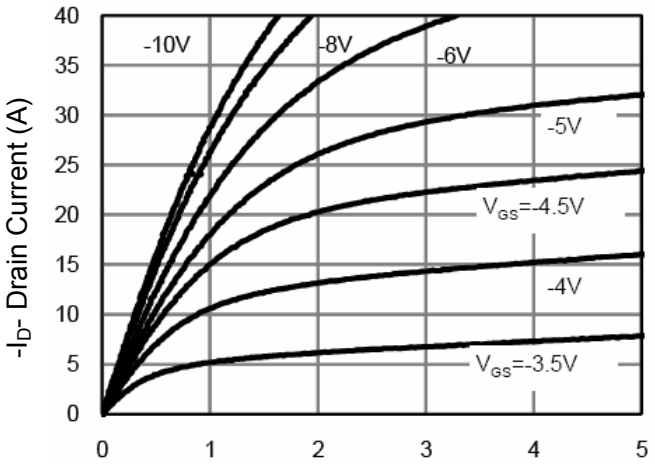


Figure 1 Output Characteristics

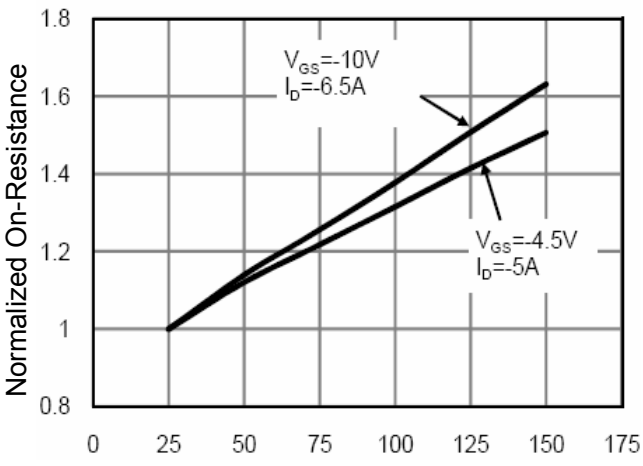


Figure 4 Rdson-Junction Temperature

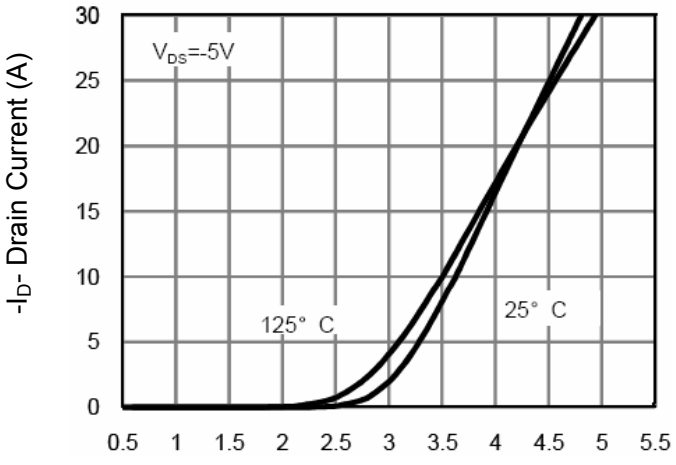


Figure 2 Transfer Characteristics

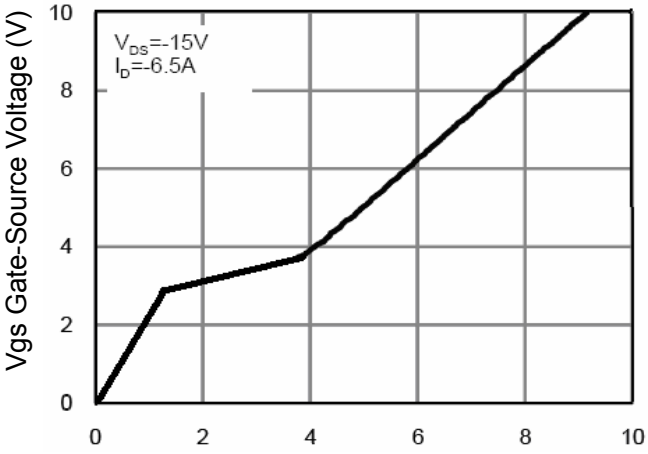


Figure 5 Gate Charge

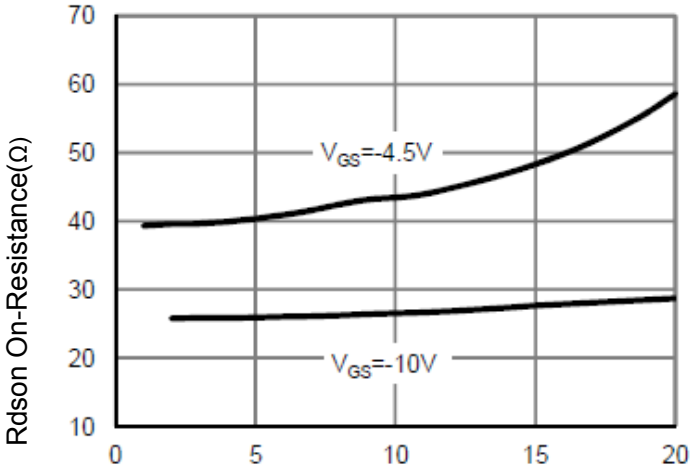


Figure 3 Rdson- Drain Current

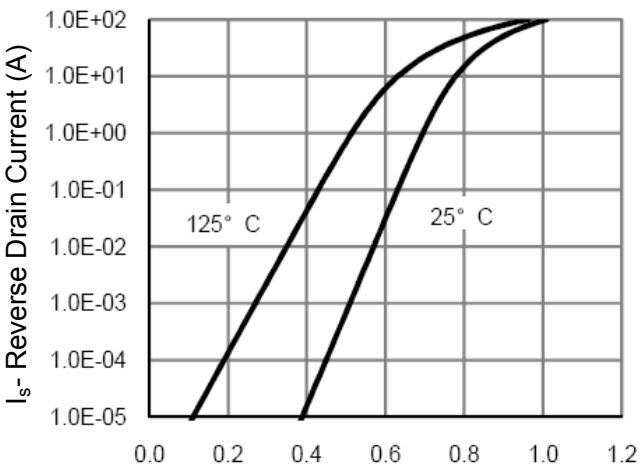


Figure 6 Source- Drain Diode Forward

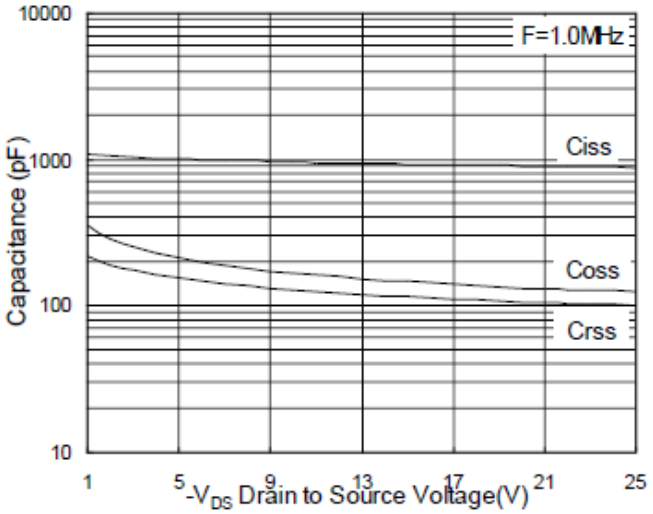
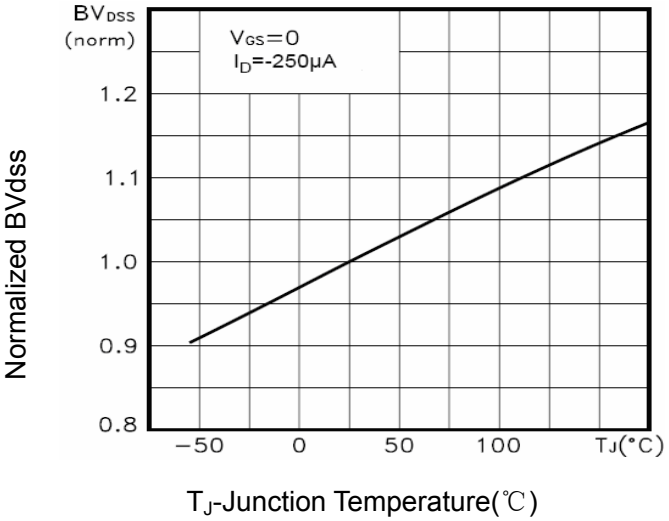
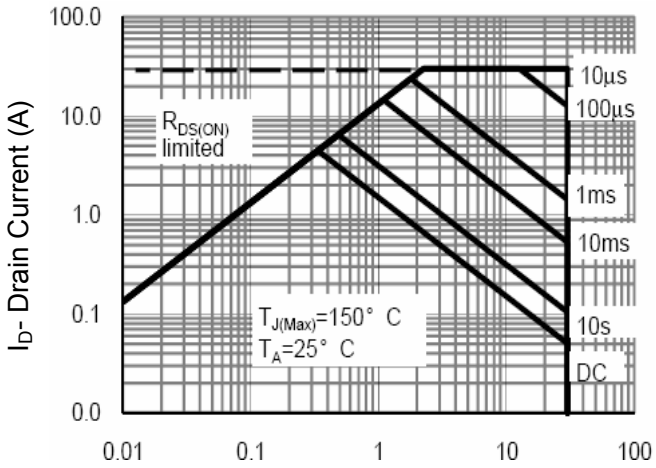


Figure 7 Capacitance vs Vds



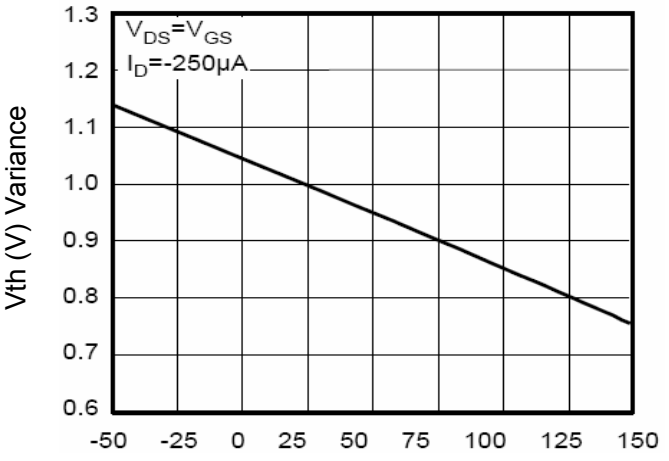
TJ-Junction Temperature(℃)

Figure 9 BV_{DSS} vs Junction Temperature



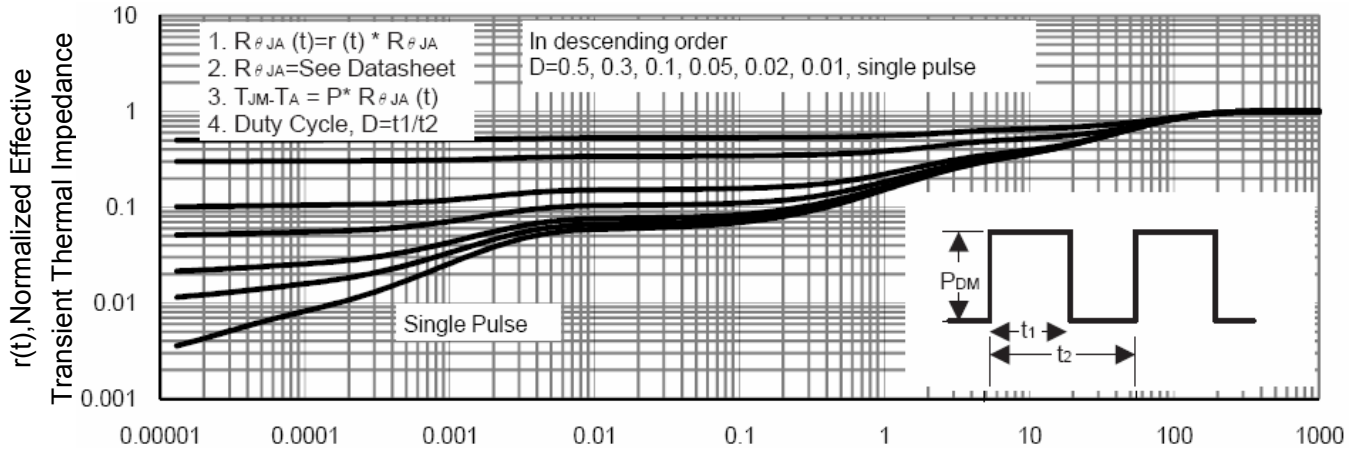
Vds Drain-Source Voltage (V)

Figure 8 Safe Operation Area



TJ-Junction Temperature(℃)

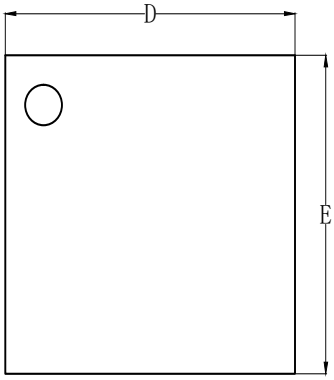
Figure 10 $V_{GS(th)}$ vs Junction Temperature

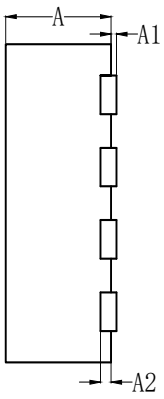


Square Wave Pluse Duration(sec)

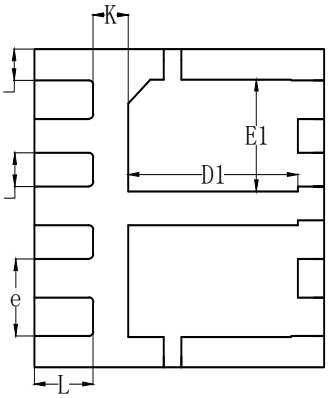
Figure 11 Normalized Maximum Transient Thermal Impedance

DFN3.3×3.3-8a PACKAGE INFORMATION





SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.05
A2	0.203 TIY		
b	0.30	—	0.45
D	3.25	3.30	3.35
D1	1.80	1.90	2.00
E	3.25	3.30	3.35
E1	1.06	1.16	1.26
E2	0.325 TIY		
e	0.75 BSC		
K	0.40 BSC		
L	0.57	0.67	0.77



E2

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