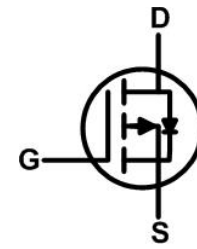




- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

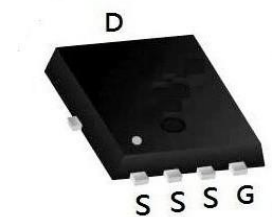


Description

The WLQ60P03D is the high cell density trenched P-ch MOSFETs, which provide excellent R_{DS(on)} and gate charge for most of the synchronous buck converter applications.

The WLQ60P03D meet the RoHS and Gree Product requirement 100% EAS guaranteed with full function reliability approved.

PDFN3333-8L Pin Configuration



Product Summary

BVDSS	R _{DS(on)}	I _D
-30V	7.5mΩ	-55A

Absolute Maximum Ratings (T_A = 25°C, unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V _{DS}	-30	V
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C =25°C	I _D	-55	A
	T _C =100°C		-30	
Pulsed Drain Current ¹		I _{DM}	-168	A
Single Pulse Avalanche Energy ²		EAS	45	mJ
Total Power Dissipation	T _C =25°C	P _D	37	W
Operating Junction and Storage Temperature Range		T _J , T _{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient ³	R _{θJA}	75	°C/W
Thermal Resistance from Junction-to-Case	R _{θJC}	3.36	°C/W



Electrical Characteristics ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30	-	-	V
Gate-body Leakage current	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 100	nA
Zero Gate Voltage Drain Current	$T_J=25^\circ\text{C}$	$V_{DS} = -30V, V_{GS} = 0V$	-	-	-1	μA
	$T_J=100^\circ\text{C}$		-	-	-100	
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.0	-	-2.5	V
Drain-Source On-Resistance ⁴	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -30A$	-	7.5	14	m Ω
		$V_{GS} = -4.5V, I_D = -15A$	-	10	22	
Forward Transconductance ⁴	g_{fs}	$V_{DS} = -5V, I_D = -30A$	-	57	-	S
Dynamic Characteristics⁵						
Input Capacitance	C_{iss}	$V_{DS} = -15V, V_{GS} = 0V, f = 1\text{MHz}$	-	2396	-	pF
Output Capacitance	C_{oss}		-	325	-	
Reverse Transfer Capacitance	C_{rss}		-	283	-	
Gate Resistance	R_g	$f = 1\text{MHz}$	-	10.5	-	Ω
Switching Characteristics⁵						
Total Gate Charge	Q_g	$V_{GS} = -10V, V_{DS} = -15V, I_D = -30A$	-	30	-	nC
Gate-Source Charge	Q_{gs}		-	5	-	
Gate-Drain Charge	Q_{gd}		-	7.5	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -10V, V_{DD} = -15V, R_G = 3\Omega, I_D = -30A$	-	14.1	-	ns
Rise Time	t_r		-	20	-	
Turn-Off Delay Time	$t_{d(off)}$		-	94	-	
Fall Time	t_f		-	65	-	
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -30A, dI/dt = 100A/\mu s$	-	19	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	9	-	nC
Drain-Source Body Diode Characteristics						
Diode Forward Voltage ⁴	V_{SD}	$I_S = -1A, V_{GS} = 0V$	-	-	-1.2	V
Continuous Source Current	$T_C=25^\circ\text{C}$	I_S	-	-	-55	A

Note :

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$.
2. The EAS data shows Max. rating . The test condition is $V_{DD} = -25V, V_{GS} = -10V, L = 0.1\text{mH}, I_{AS} = -30A$.
3. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. This value is guaranteed by design hence it is not included in the production test.



Typical Characteristics

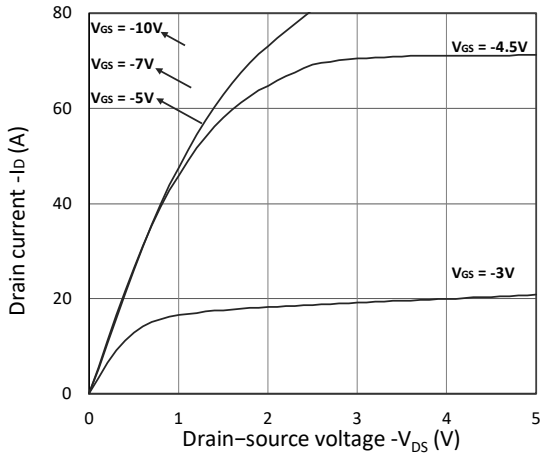


Figure 1. Output Characteristics

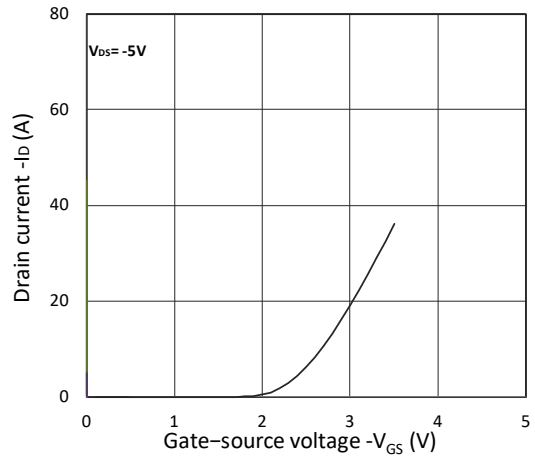


Figure 2. Transfer Characteristics

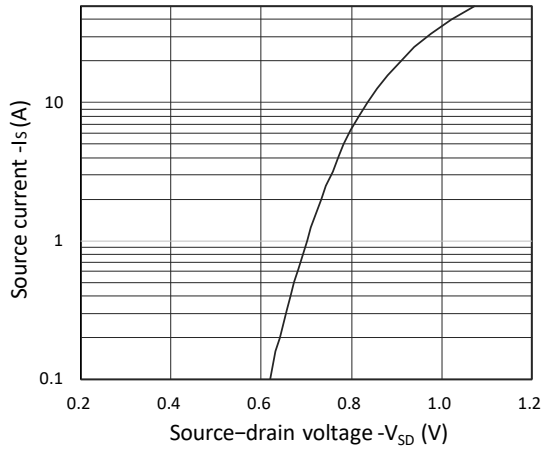


Figure 3. Forward Characteristics of Reverse

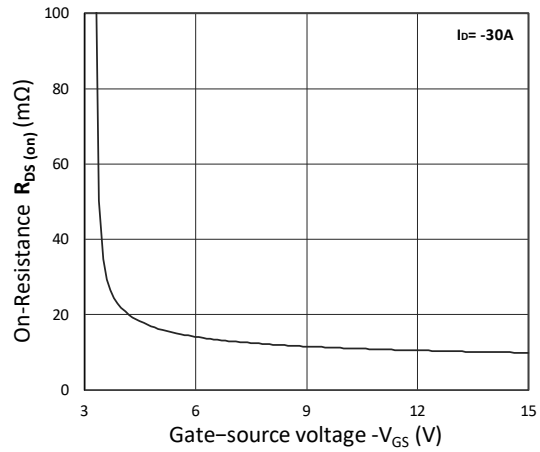


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

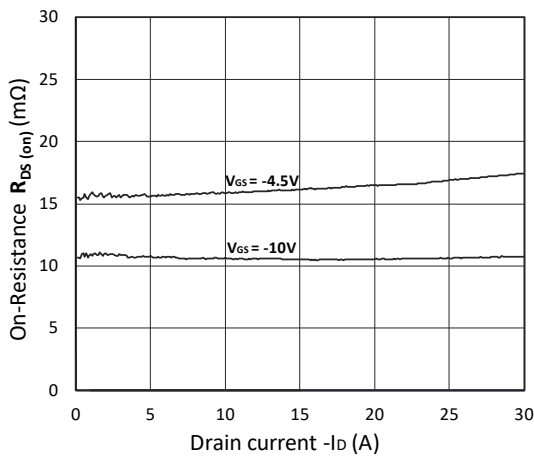


Figure 5. $R_{DS(ON)}$ vs. I_D

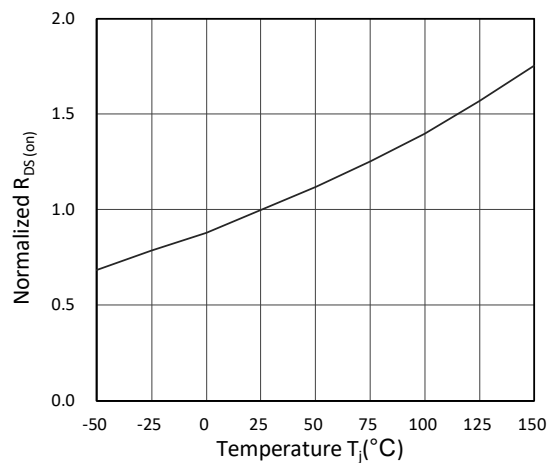


Figure 6. Normalized $R_{DS(ON)}$ vs. Temperature

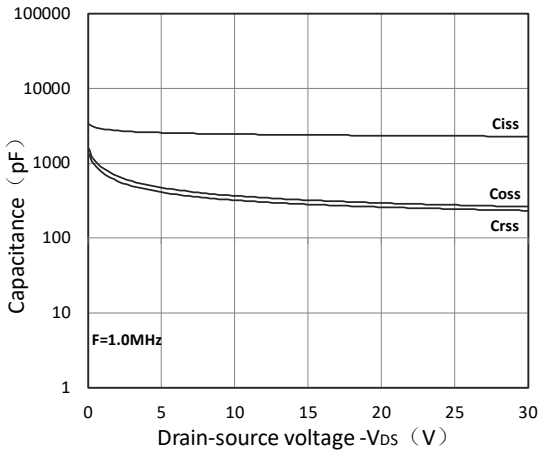


Figure 7. Capacitance Characteristics

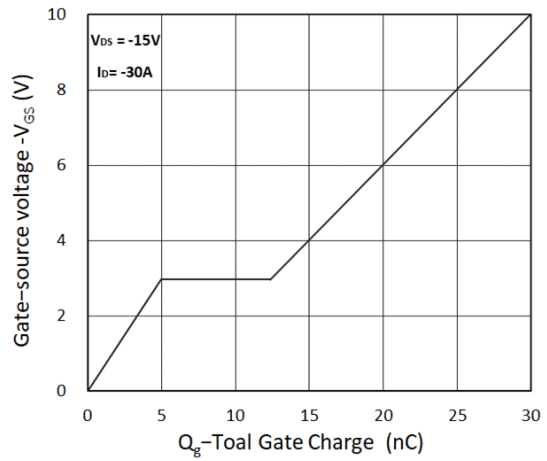


Figure 8. Gate Charge Characteristics

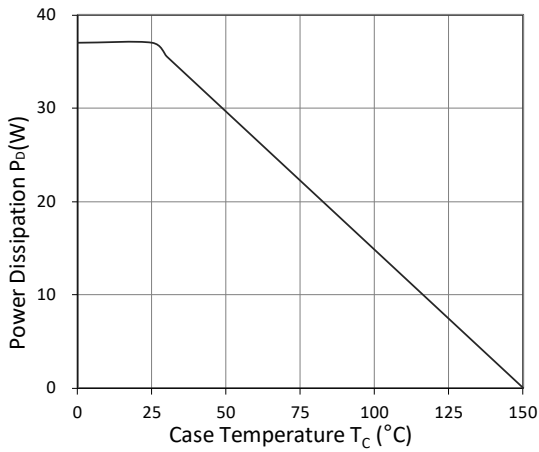


Figure 9. Power Dissipation

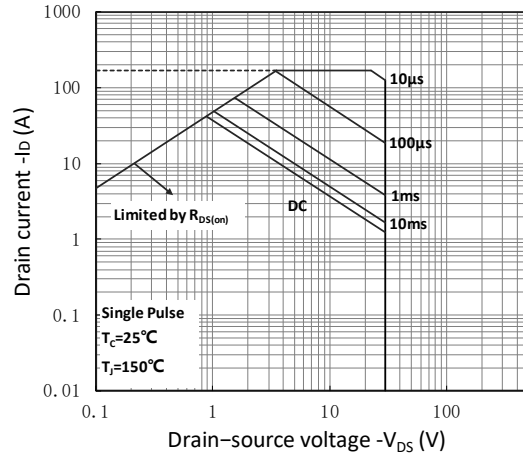


Figure 10. Safe Operating Area

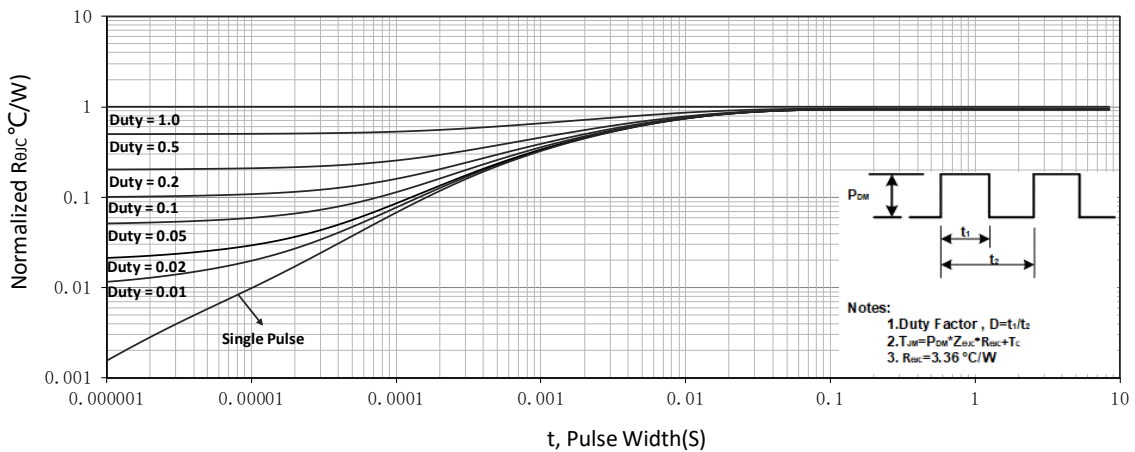
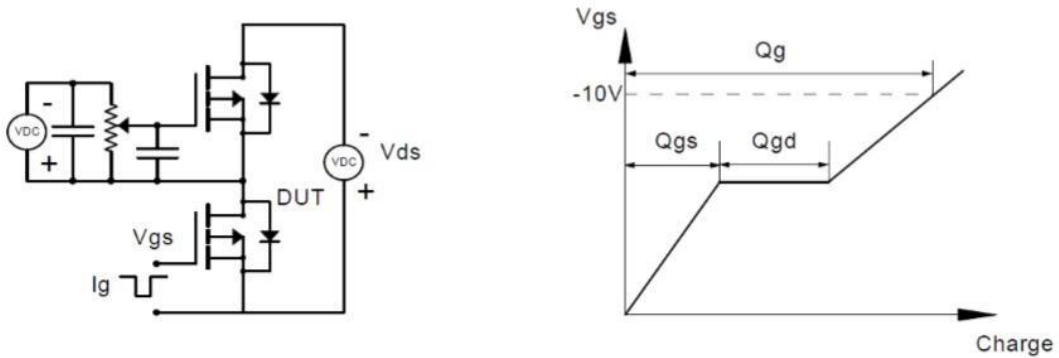


Figure 11. Normalized Maximum Transient Thermal Impedance

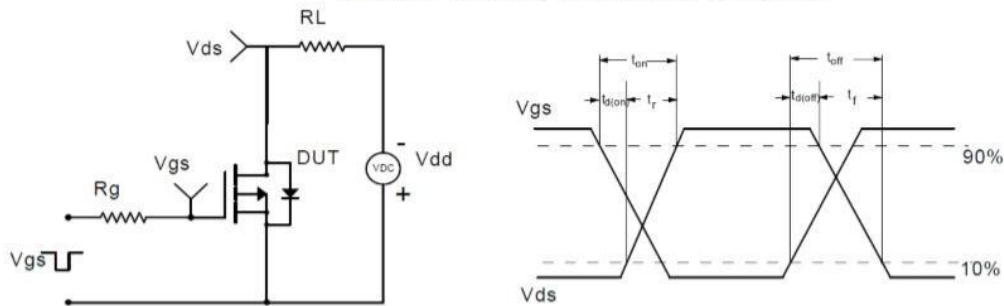


Test Circuit

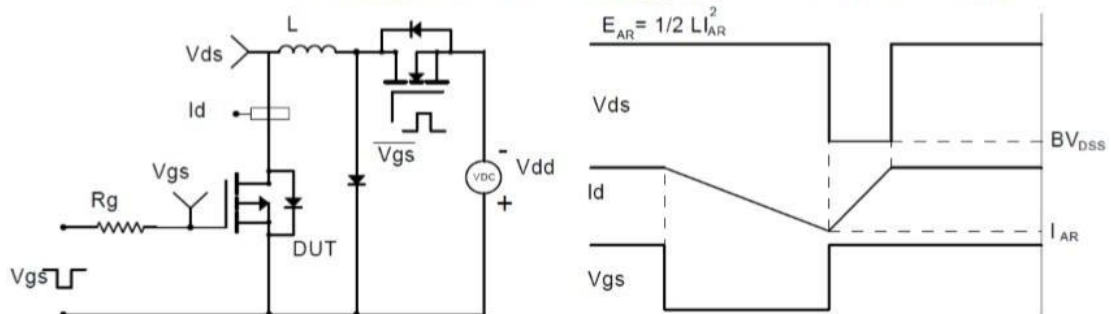
Gate Charge Test Circuit & Waveform



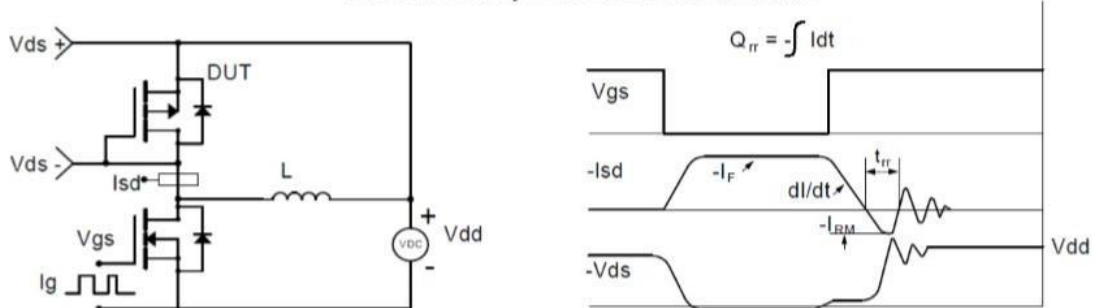
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

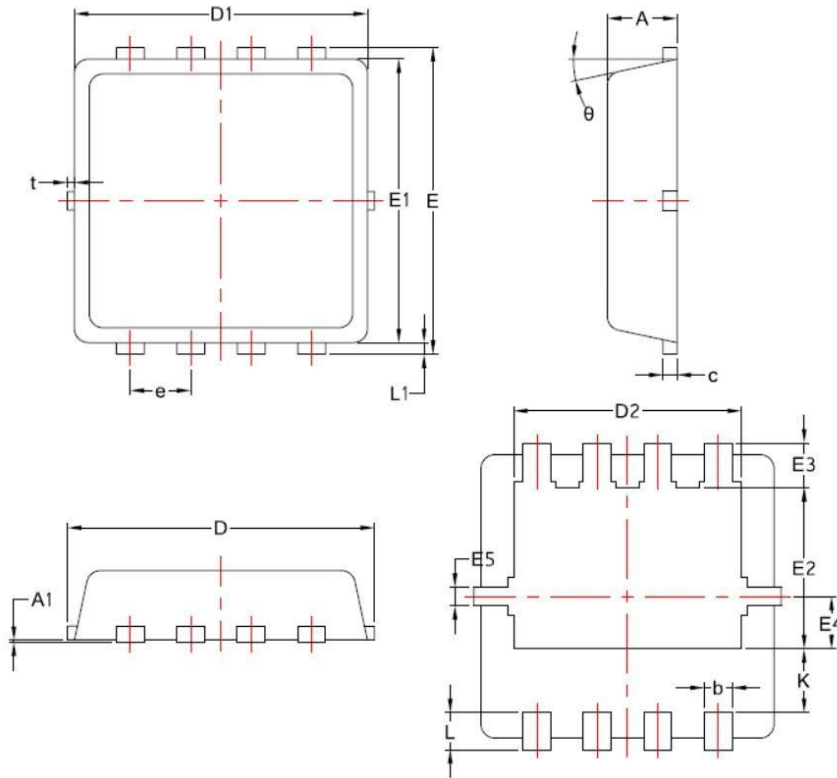


Diode Recovery Test Circuit & Waveforms





Package Mechanical Data- PDFN3.3X3.3-8L



SYMBOL	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
θ	10°	12°	14°



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