



Description

The Power MOSFET is fabricated using the advanced planar VDMOS technology. The resulting device has low conduction resistance, superior switching performance and high avalanche energy.

Features

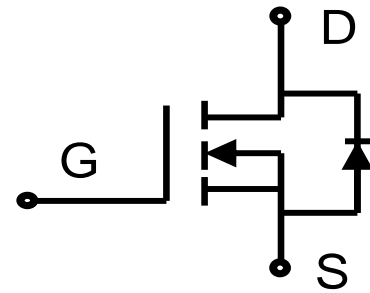
- ◆ Low $R_{DS(on)}$
- ◆ Low gate charge (typ. $Q_g = 77nC$)
- ◆ 100% UIS tested
- ◆ RoHS compliant

Applications

- ◆ Power factor correction.
- ◆ Switched mode power supplies.

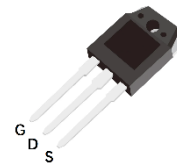
Product Summary

V_{DSS}	500V
I_D	25A
$R_{DS(on),max}$	0.2 Ω
$Q_{g,typ}$	77nC



N-Channel MOSFET

Pin Configuration



TO-3P

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	500	V
Continuous drain current ($T_C = 25^\circ C$) ($T_C = 100^\circ C$)	I_D	25	A
		18.6	A
Pulsed drain current ¹⁾	I_{DM}	100	A
Gate-Source voltage	V_{GSS}	± 30	V
Avalanche energy, single pulse ²⁾	E_{AS}	1280	mJ
Power Dissipation ($T_C = 25^\circ C$)	P_D	403	W
Operating junction and storage temperature range	T_J, T_{STG}	-55 to +150	$^\circ C$
Continuous diode forward current	I_S	25	A
Diode pulse current	$I_{S,pulse}$	100	A

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, Junction-to-case	$R_{\theta JC}$	0.31	$^\circ C/W$
Thermal resistance, Junction-to-ambient ³⁾	$R_{\theta JA}$	58.18	$^\circ C/W$
Soldering temperature, wavesoldering only allowed at leads. (1.6mm from case for 10s)	T_{solid}	260	$^\circ C$



Package Marking and Ordering Information

Device	Device Package	Marking	Units/Tube
WLP25N60EP	TO-3P	WLP25N60EP	30

Electrical Characteristics

$T_c = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0\text{ V}, I_D=0.25\text{ mA}$	500	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=0.25\text{ mA}$	2	-	4	V
Drain cut-off current	I_{DSS}	$V_{DS}=500\text{ V}, V_{GS}=0\text{ V},$ $T_j = 25^\circ\text{C}$ $T_j = 125^\circ\text{C}$	-	-	1 100	μA
Gate leakage current, Forward	I_{GSSF}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	-	100	nA
Gate leakage current, Reverse	I_{GSSR}	$V_{GS}=-20\text{ V}, V_{DS}=0\text{ V}$	-	-	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=12.5\text{ A}$	-	0.16	0.2	Ω
Dynamic characteristics						
Input capacitance	C_{iss}	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V},$ $f = 250\text{ kHz}$	-	3901	-	pF
Output capacitance	C_{oss}		-	91	-	
Reverse transfer capacitance	C_{rss}		-	10.6	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 29\text{ A}$ $R_G = 10\ \Omega, V_{GS}=10\text{ V}$	-	37.9	-	ns
Rise time	t_r		-	104.0	-	
Turn-off delay time	$t_{d(off)}$		-	90.1	-	
Fall time	t_f		-	20.5	-	
Gate charge characteristics						
Gate to source charge	Q_{gs}	$V_{DD}=400\text{ V}, I_D=29\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	18.5	-	nC
Gate to drain charge	Q_{gd}		-	27.5	-	
Gate charge total	Q_g		-	77.8	-	
Gate plateau voltage	$V_{plateau}$		-	4.8	-	V
Reverse diode characteristics						
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=25\text{ A}$	-	-	1.3	V
Reverse recovery time	t_{rr}	$V_R=400\text{ V}, I_F=29\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	385.7	-	ns
Reverse recovery charge	Q_{rr}		-	5.6	-	μC
Peak reverse recovery current	I_{rrm}		-	22.9	-	A

Notes:

- Pulse width limited by maximum junction temperature.
- $I_{AS}=16\text{ A}, L=10\text{ mH}, V_{DD}=60\text{ V},$ Starting $T_j=25^\circ\text{C}$.
- The value of R_{thJA} is measured by placing the device in a still air box which is one cubic foot.



Electrical Characteristics Diagrams

Figure 1. Typ. Output Characteristics

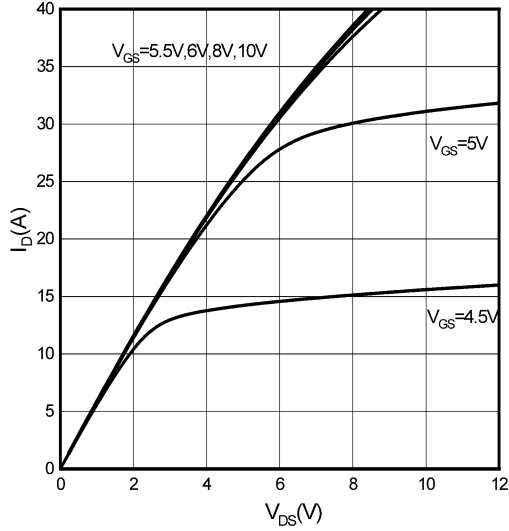


Figure 2. Transfer Characteristics

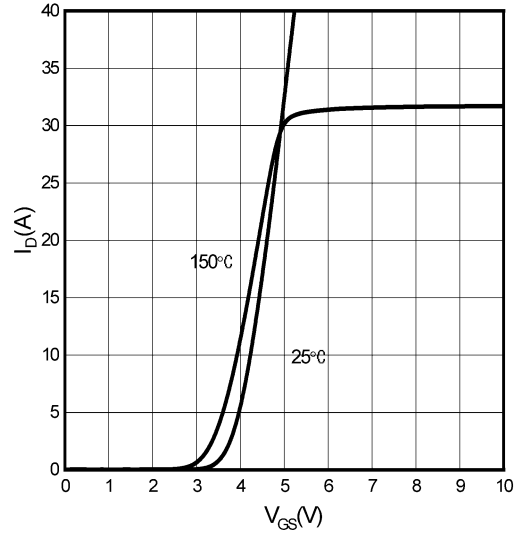


Figure 3. On-Resistance vs. Drain Current

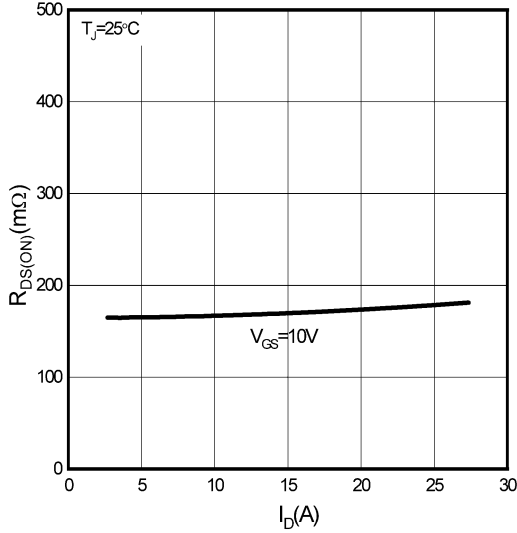


Figure 4. On-Resistance vs. Temperature

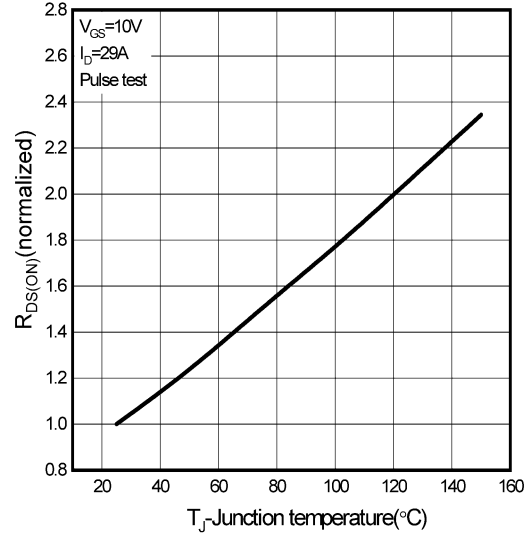


Figure 5. Breakdown Voltage vs. Temperature

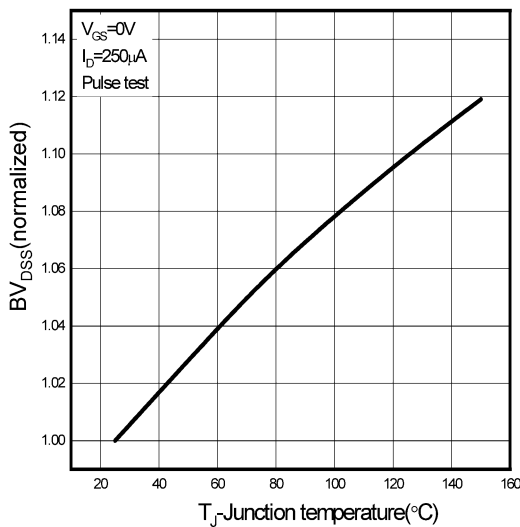


Figure 6. Threshold Voltage vs. Temperature

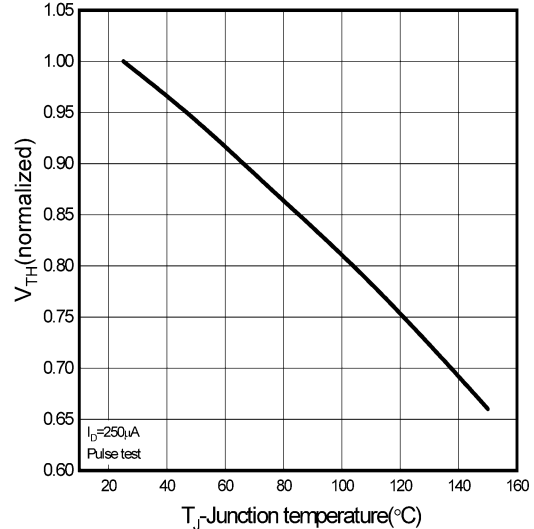




Figure 7. $R_{DS(on)}$ vs. Gate Voltage

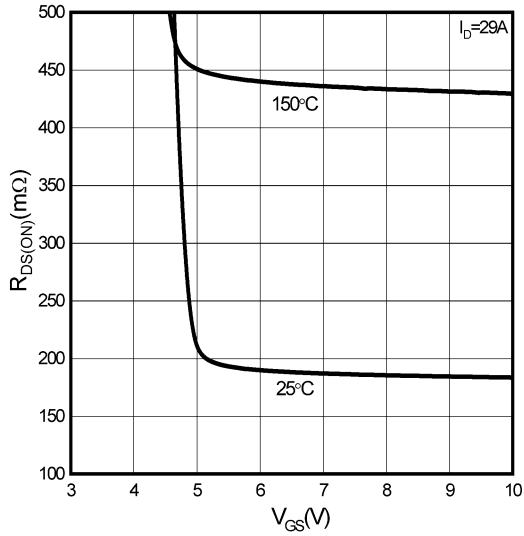


Figure 8. Body-Diode Characteristics

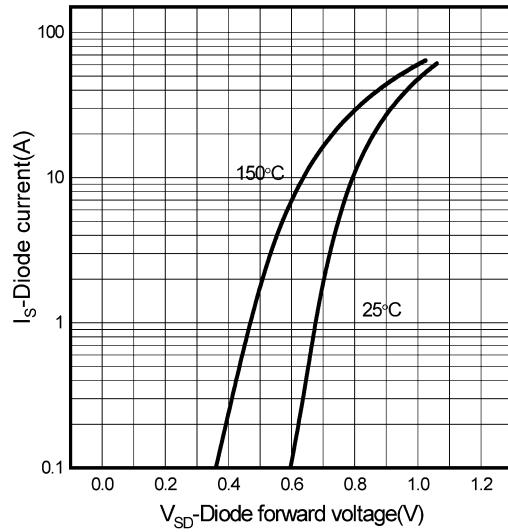


Figure 9. Capacitance Characteristics

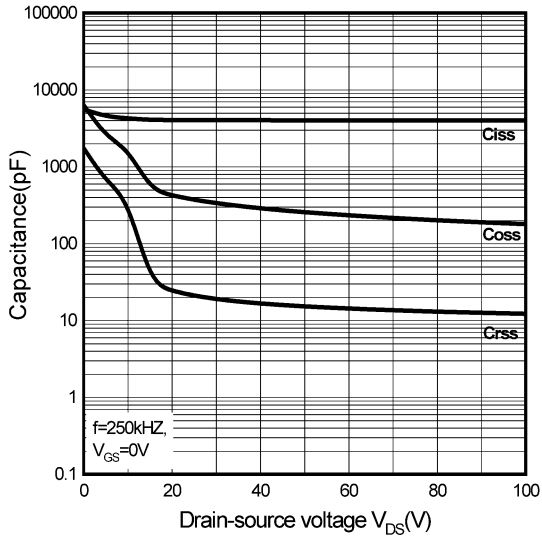


Figure 10. Gate Charge Characteristics

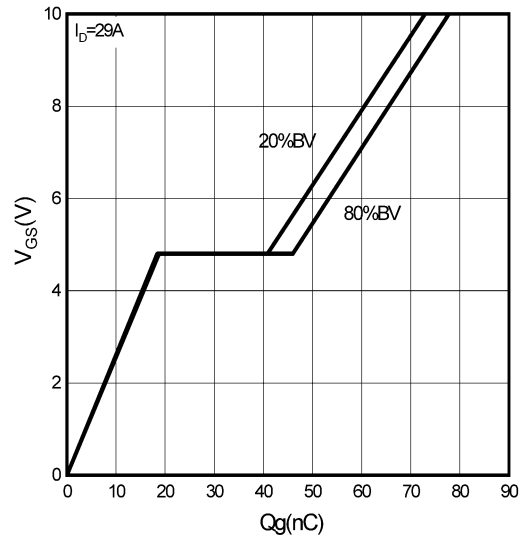


Figure 11. Drain Current Derating

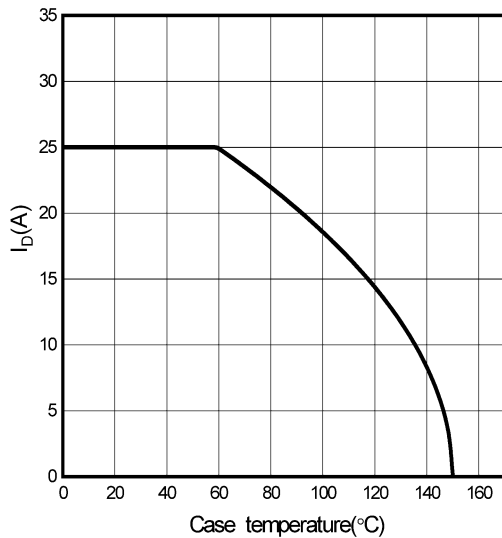


Figure 12. Power Dissipation vs. Temperature

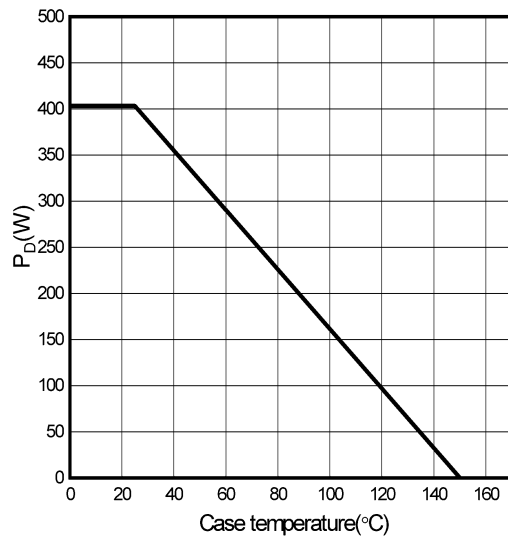




Figure 13. Safe Operating Area

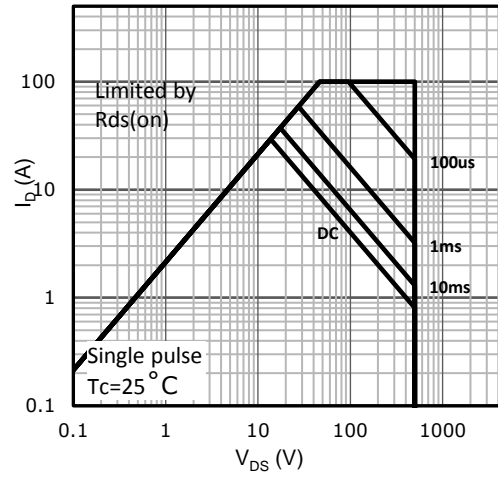
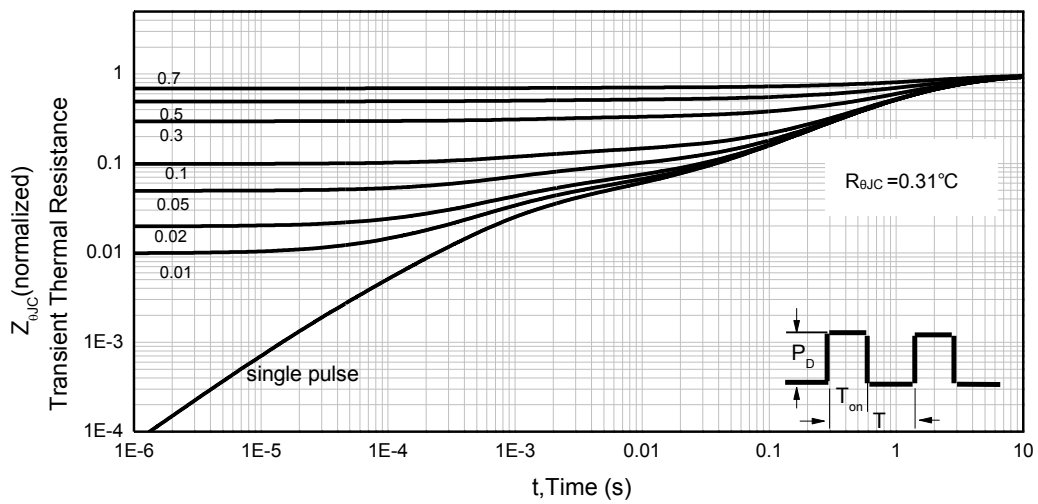


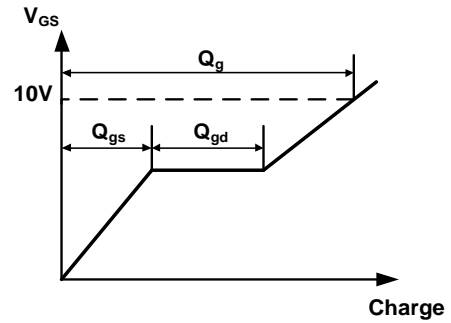
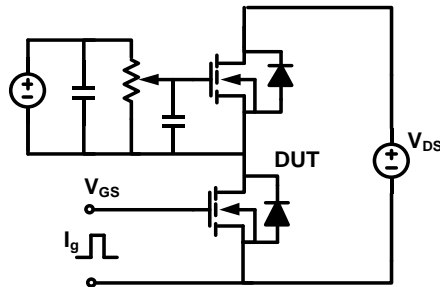
Figure 14. Normalized Maximum Transient Thermal Impedance (R_{thJC})



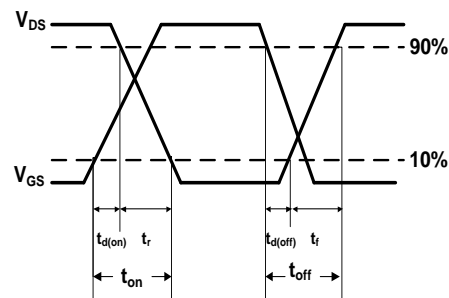
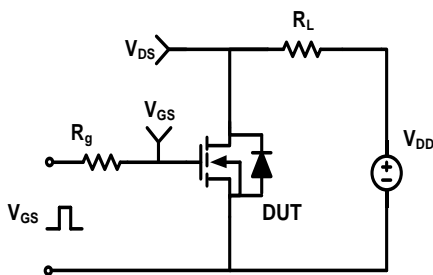


Test Circuit & Waveforms

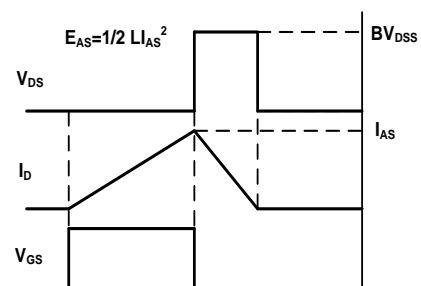
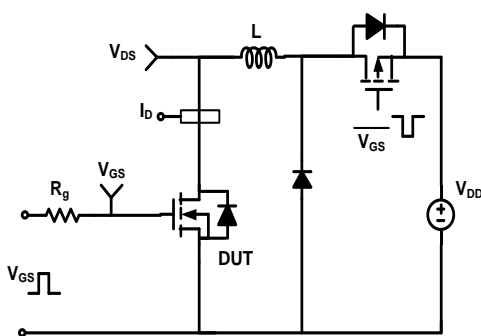
Gate Charge Test Circuit & Waveform



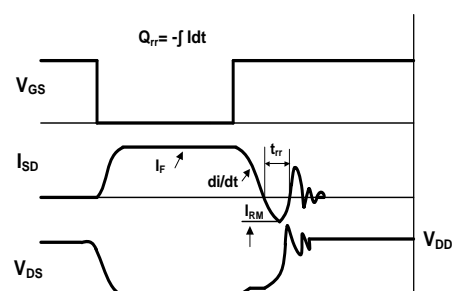
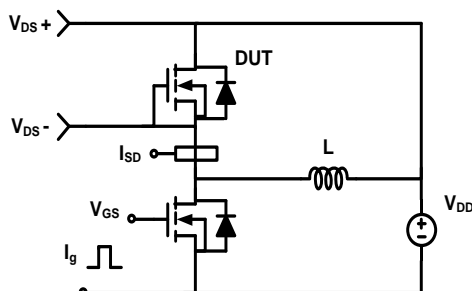
Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveform



Diode Recovery Test Circuit & Waveform





Mechanical Dimensions for TO-3P

