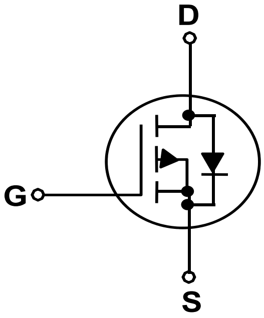
WLP60P80

60V P-Channel Power MOSFET

General Description

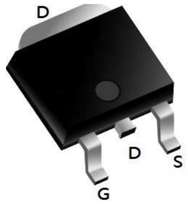
This Power MOSFET is produced using Maple semi's advanced TRENCH technology.
This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.



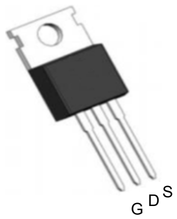
Application

PWM Application
Load Switch
Power Management

TO-252



TO-220



Features

- P-Channel: -60V - 80A
  $R_{DS(on)Typ}$= 16.5mΩ@V_{GS} = -10 V
  $R_{DS(on))Typ}$= 18.5mΩ@V_{GS} = -4.5V
- Very Low On-resistance RDS(ON)
- LowCrss
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	WL80P06/50P06	Units
V_{DSS}	Drain-Source Voltage	-60	V
I_D	Drain Current - Continuous (T_C = 25℃)	-80	A
	- Continuous (T_C = 100℃)	-64	A
I_{DM}	Drain Current - Pulsed (Note 1)	-320	A
V_{GSS}	Gate-Source Voltage	±20	V
E_{AS}	Single Pulsed Avalanche Energy	756	mJ
P_D	Power Dissipation (T_C = 25℃)	270	W
$R_{θJC}$	Thermal Resistance, Junction to Case	0.46	W/℃
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	℃

* Drain current limited by maximum junction temperature.

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 uA	-60	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -60 V, V_{GS} = 0 V	--	--	-1	uA
		V_{DS} = -48V, T_C = 125℃	--	--	-10	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20V, V_{DS} = 0 V	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 uA	-1.1	-1.6	-2.2	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -20A	--	16.5	19.5	mΩ
		V_{GS} = -4.5 V, I_D = -20A	-	18.5	22	

Dynamic Characteristics

C_{iss}	Input Capacitance	V_{DS} = -20 V, V_{GS} = 0 V, f = 1.0 MHz	--	4400	-	pF
C_{oss}	Output Capacitance		--	259	-	pF
C_{rss}	Reverse Transfer Capacitance		--	212	-	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	V_{GS}= -10 V, V_{DS}= -30 V, R_G =1Ω ,I_D= -20A	--	24	--	ns
t_r	Turn-On Rise Time		--	18	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	56	--	ns
t_f	Turn-Off Fall Time		--	30	--	ns
Q_g	Total Gate Charge	V_{DS} = -30 V, I_D = -20A, V_{GS} = -10V	--	115	--	nC
Q_{gs}	Gate-Source Charge		--	27.4	--	nC
Q_{gd}	Gate-Drain Charge		--	50	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	-80	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-320	A
V_{SD}	Drain to Source Diode Forward Voltage, V_{GS} = 0V, I_{SD} = -20A, T_J = 25℃		--	--	-1.2	V
t_{rr}	Reverse Recovery Time T_J = 25°C, IF =-20A,di/dt =100A/μs		--	117	-	nS
Q_{rr}	Reverse Recovery Charge T_J = 25°C, IF =-20A,di/dt =100A/μs		--	420	-	nC

Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: T_J =25℃, VDD =-25V, VG =-5V, RG =25Ω, L=0.5mH, I_{AS}
3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

P- Channel Typical Characteristics

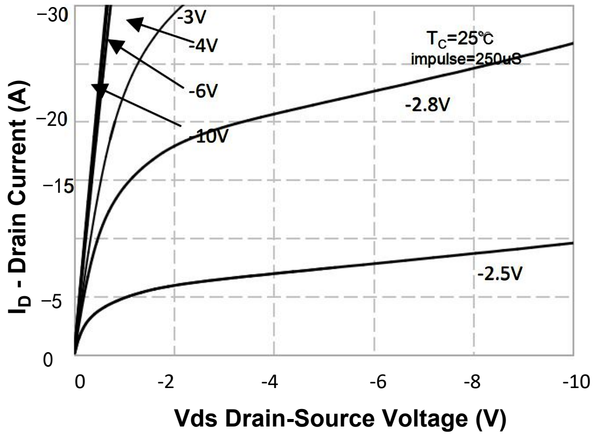


Figure 1. On-Region Characteristics

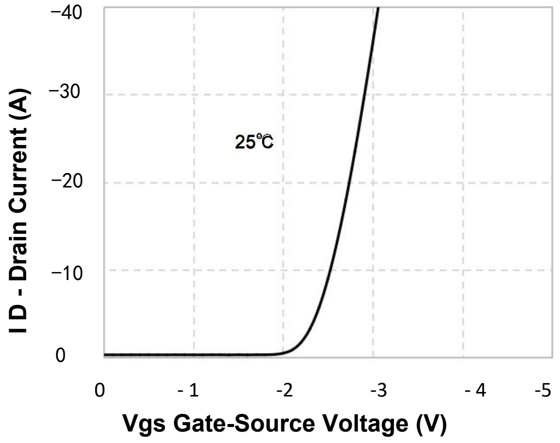


Figure 2. Transfer Characteristics

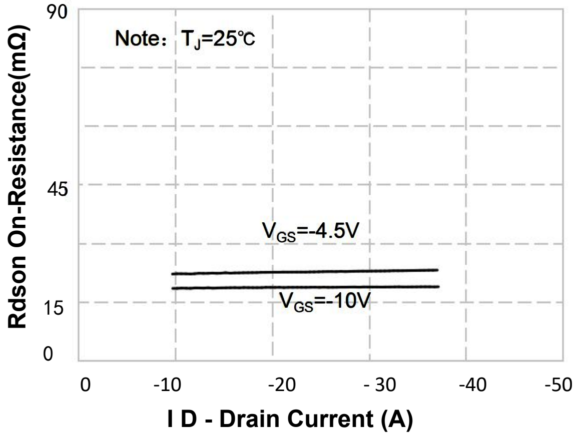


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

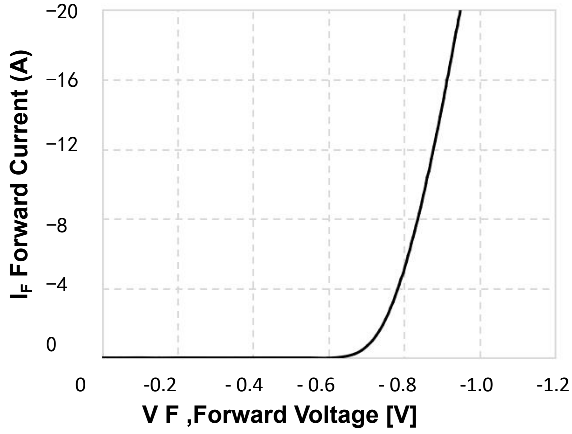


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

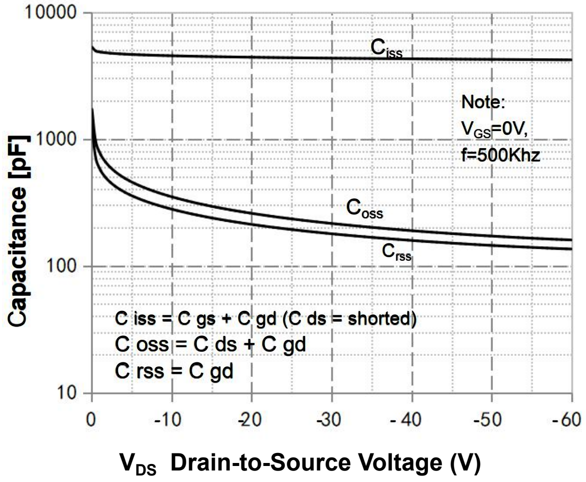


Figure 5. Capacitance Characteristics

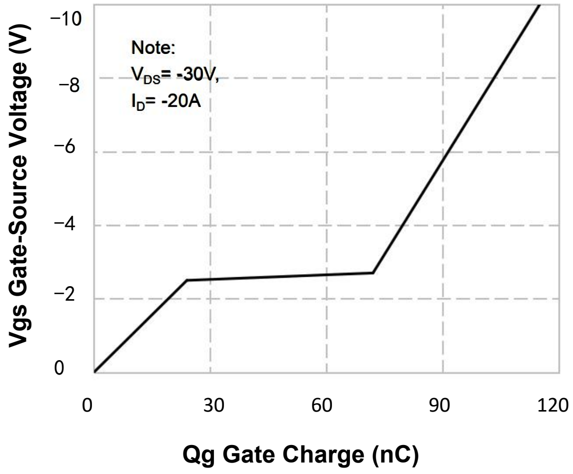


Figure 6. Gate Charge Characteristics

P- Channel Typical Characteristics (Continued)

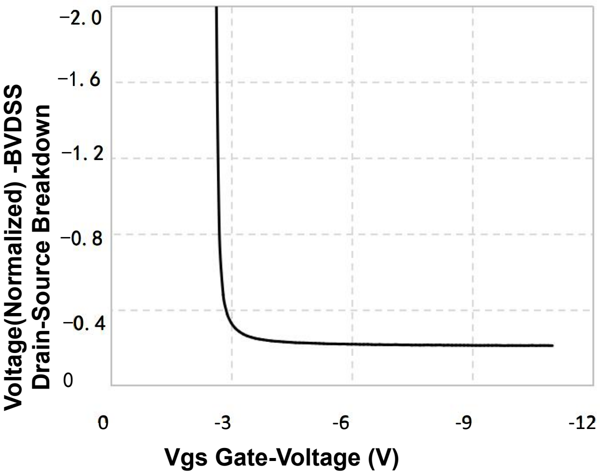


Figure 7. Breakdown Voltage Variation vs Gate-Voltage

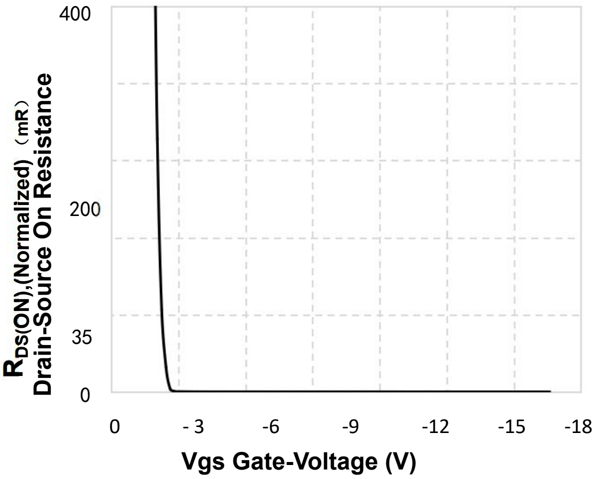


Figure 8. On-Resistance Variation vs Gate Voltage

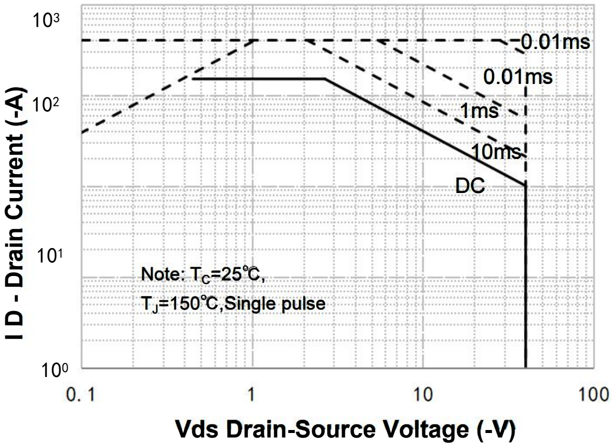


Figure 9. Maximum Safe Operating Area

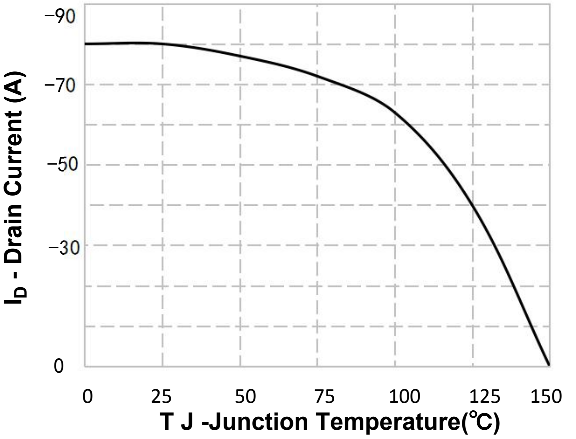


Figure 10. Maximum PContinuous Drain Currentvs Case Temperature

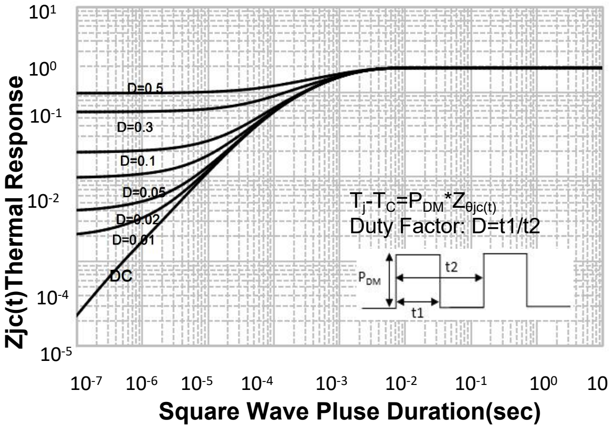
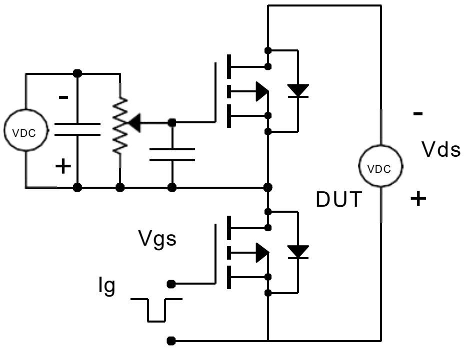
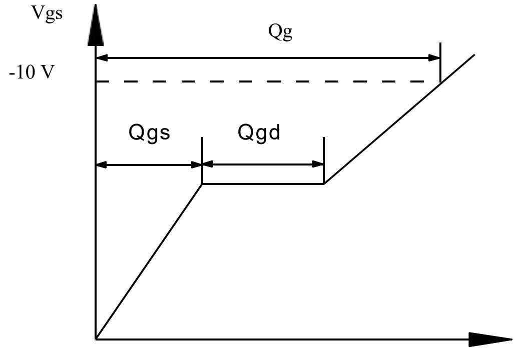


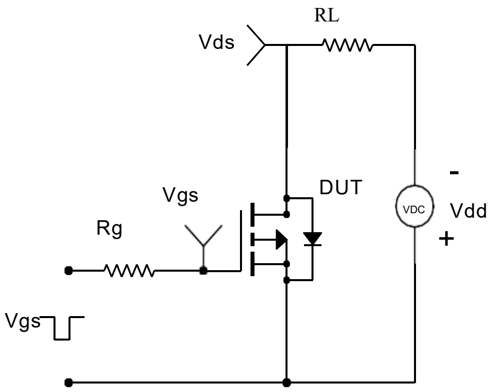
Figure 11. Transient Thermal Response Curve

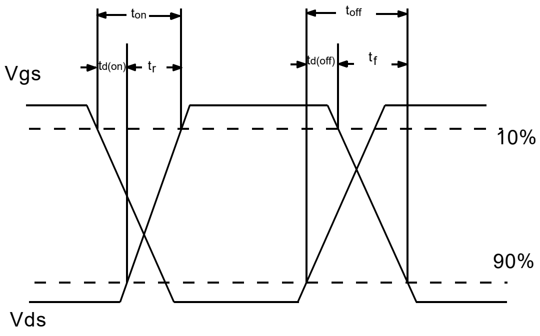
Gate Charge Test Circuit & Waveform



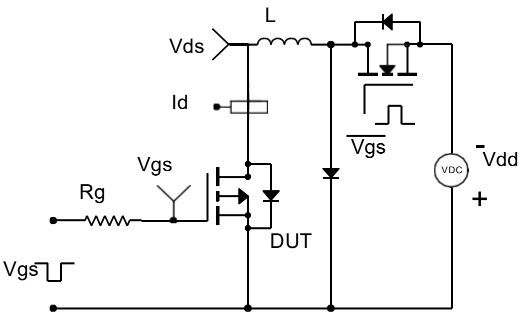


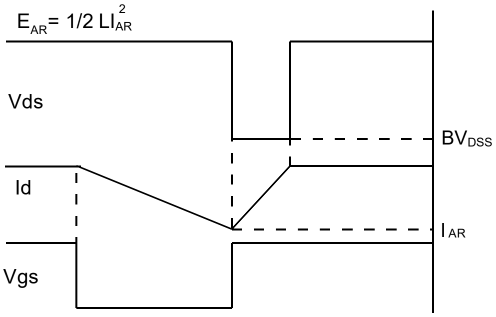
Resistive Switching Test Circuit & Waveforms



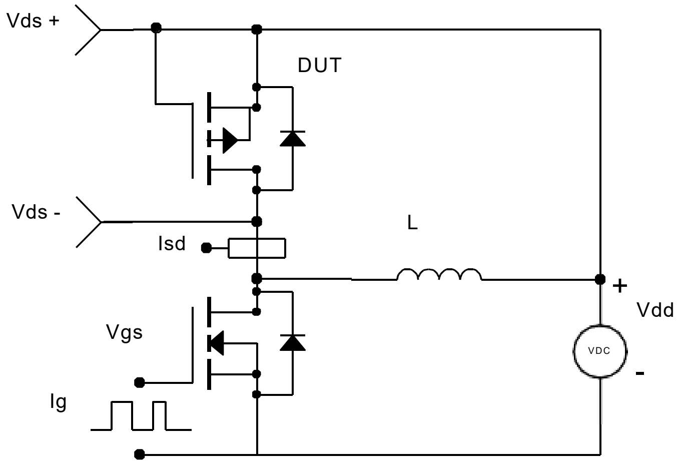


Unclamped Inductive Switching Test Circuit & Waveforms

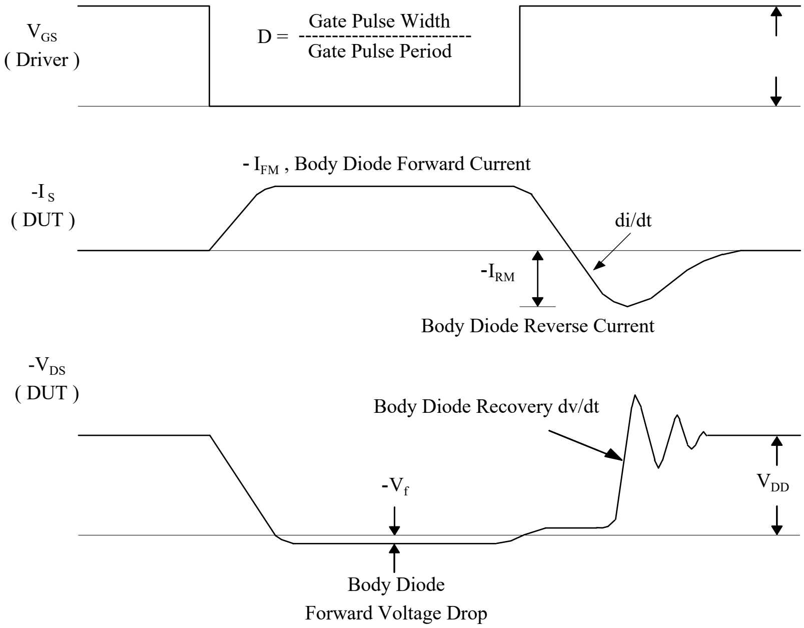




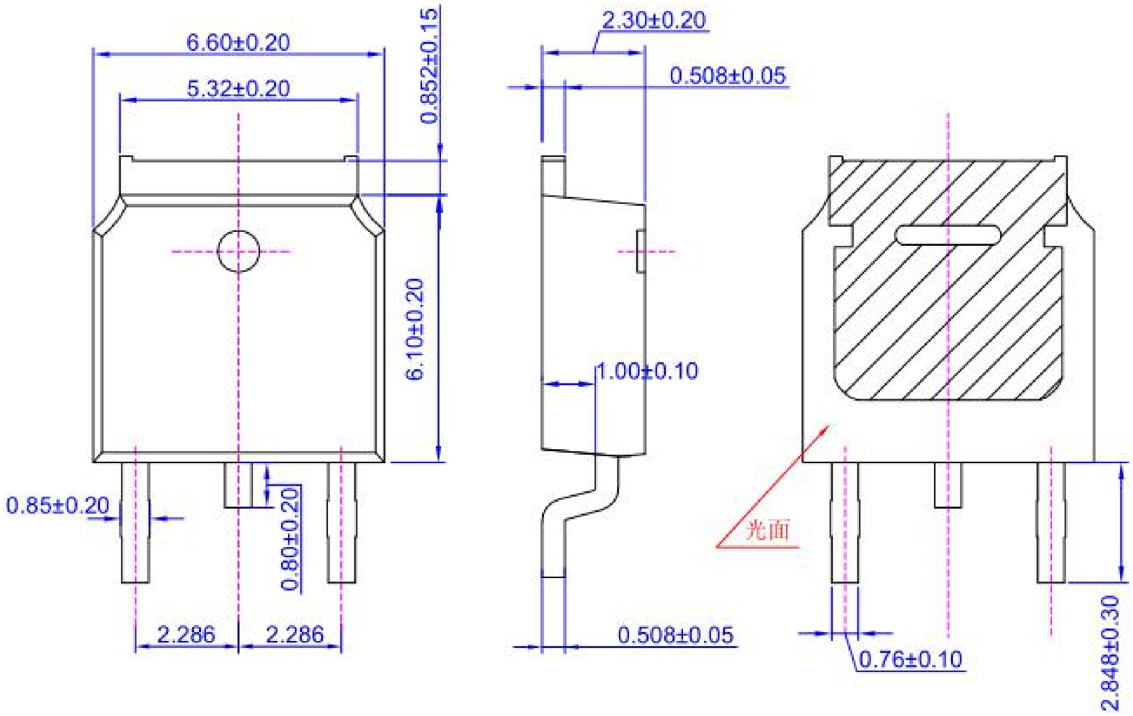
Peak Diode Recovery dv/dt Test Circuit & Waveforms

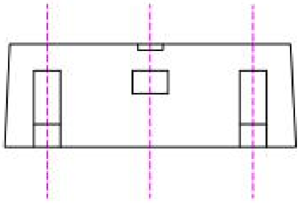


- dv/dt controlled by R_G
- I_{SD} controlled by pulse period



TO-252 OUTLINE



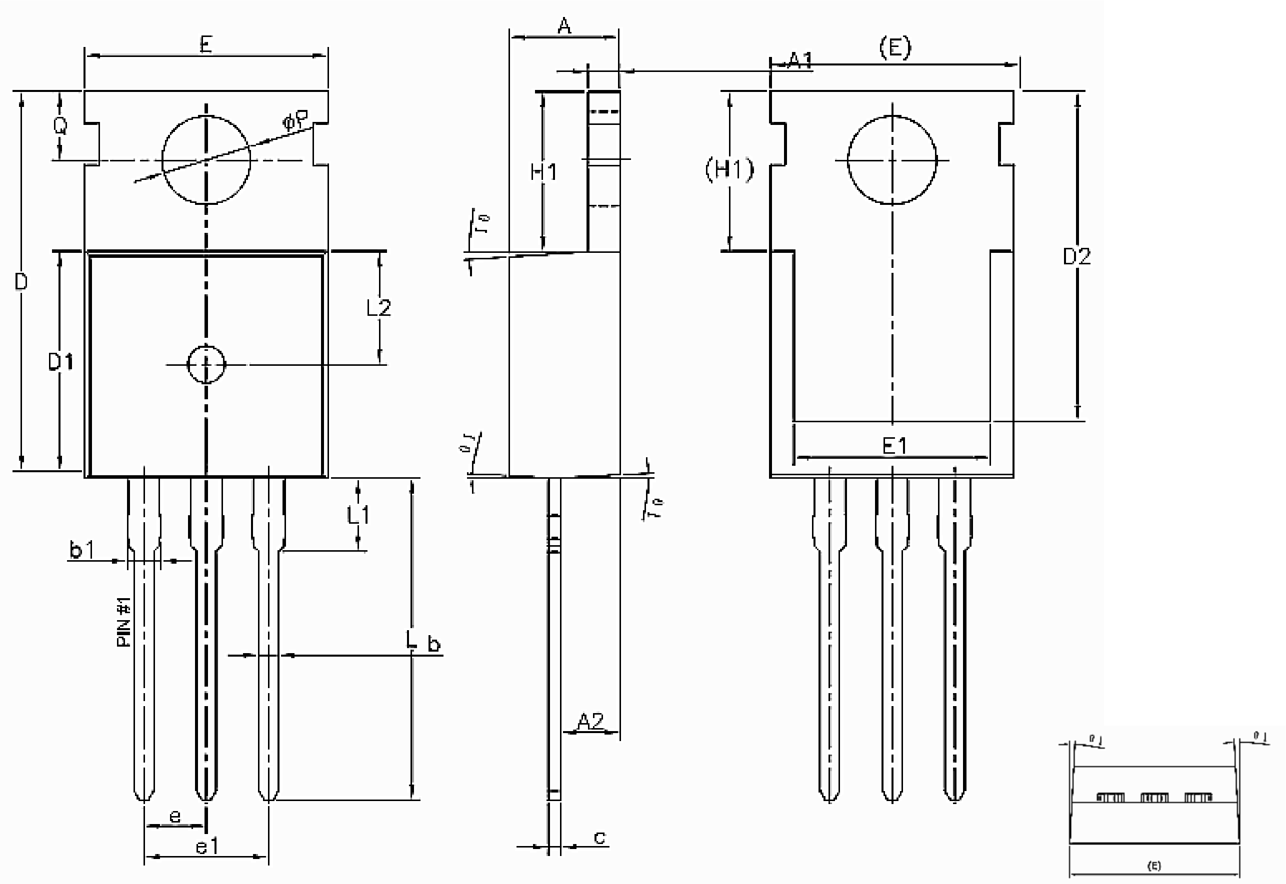


NOTE：

1The plastic package is not marked as smooth surfaceRa=0.1;Subglossy surfaceRa=0.8

2.Undeclared tolerance±0.25,Unmarked filletRmax=0.25

Outlines TO-220 Package



Unit:mm			
Symbol	**Min.**	**Nom**	**Max.**
A	4.40	4.50	4.60
A1	1.27	1.30	1.33
A2	2.30	2.40	2.50
b	0.70	---	0.90
b2	1.27	---	1.40
c	0.45	0.50	0.60
D	15.30	15.70	16.10
D1	9.10	9.20	9.30
D2	13.10	---	13.70
E	9.70	9.90	10.20

Unit:mm			
Symbol	**Min.**	**Nom**	**Max.**
E1	7.80	8.00	8.20
e	2.54 BSC		
e1	5.08 BSC		
H1	6.30	6.50	6.70
L	12.78	13.08	13.38
L1	---	---	3.50
L2	4.60 REF		
ΦP	3.55	3.60	3.65
Q	2.73	---	2.87
θ1	1°	3°	5°

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