



Description

WENLAI Power MOSFET is fabricated using advanced super junction technology. The resulting device has extremely low on resistance, making it especially suitable for applications which require superior power density and outstanding efficiency.

Features

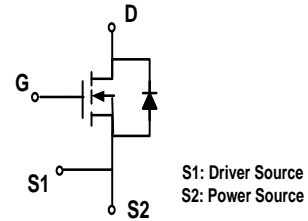
- ◆ Ultra low $R_{DS(on)}$
- ◆ Ultra low gate charge (typ. $Q_g = 16.9nC$)
- ◆ 100% UIS tested
- ◆ RoHS compliant

Applications

- ◆ Power factor correction (PFC).
- ◆ Switched mode power supplies (SMPS).
- ◆ Uninterruptible power supply (UPS).

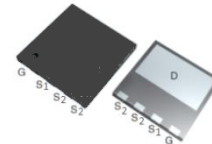
Product Summary

$V_{DS} @ T_{j,max}$	700V
$R_{DS(on),max}$	0.38Ω
I_{DM}	33A
$Q_{g,typ}$	16.9 nC



N-Channel MOSFET

Pin Configuration



DFN8×8

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	650	V
Continuous drain current ¹⁾ ($T_C = 25^\circ C$) ($T_C = 100^\circ C$)	I_D	11	A
		7	A
Pulsed drain current ²⁾	I_{DM}	33	A
Gate-Source voltage	V_{GSS}	± 30	V
Avalanche energy, single pulse ³⁾	E_{AS}	245	mJ
Power Dissipation	P_D	66	W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$
Continuous diode forward current	I_S	11	A
Diode pulse current	$I_{S,pulse}$	33	A

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.9	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient ⁴⁾	$R_{\theta JA}$	65	$^\circ C/W$
Soldering temperature, wavesoldering only allowed at leads.	T_{sold}	260	$^\circ C$



Package Marking and Ordering Information

Device	Device Package	Marking	Units/ Reel
WLQ038R650	DFN 8×8	WLQ038R650	3000

Electrical Characteristics

$T_c = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=0.25mA$	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=0.25mA$	2.5	3.5	4.5	V
Drain cut-off current	I_{DSS}	$V_{DS}=650V, V_{GS}=0V, T_j = 25^\circ\text{C}$	-	-	0.6	μA
Gate leakage current, Forward	I_{GSSF}	$V_{GS}=30V, V_{DS}=0V$	-	-	100	nA
Gate leakage current, Reverse	I_{GSSR}	$V_{GS}=-30V, V_{DS}=0V$	-	-	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=5.5A$	-	-	-	Ω
		$T_j = 25^\circ\text{C}$	-	0.33	0.38	
		$T_j = 150^\circ\text{C}$	-	0.85	-	
Gate resistance	R_G	$f=1\text{MHz, open drain}$	-	5.7	-	Ω
Dynamic characteristics						
Input capacitance	C_{iss}	$V_{DS} = 100V, V_{GS} = 0V,$ $f = 250\text{kHz}$	-	861	-	μF
Output capacitance	C_{oss}		-	33.6	-	
Reverse transfer capacitance	C_{rss}		-	1.2	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 400V, I_D = 5.5A$ $R_G = 10\Omega, V_{GS}=15V$	-	21.6	-	ns
Rise time	t_r		-	24	-	
Turn-off delay time	$t_{d(off)}$		-	59	-	
Fall time	t_f		-	7.2	-	
Gate charge characteristics						
Gate to source charge	Q_{gs}	$V_{DD}=520V, I_D=5.5A,$ $V_{GS}=0\text{ to }10V$	-	4.9	-	nC
Gate to drain charge	Q_{gd}		-	6.7	-	
Gate charge total	Q_g		-	16.9	-	
Gate plateau voltage	$V_{plateau}$		-	6	-	V
Reverse diode characteristics						
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=5.5A$	-	1.2	-	V
Reverse recovery time	t_{rr}	$V_R=400V, I_F=5.5A,$ $dI_F/dt=100\text{A}/\mu\text{s}$	-	230	-	ns
Reverse recovery charge	Q_{rr}		-	2.28	-	μC
Peak reverse recovery current	I_{rrm}		-	19.8	-	A

Notes:

- Limited by maximum junction temperature and duty cycle.
- Limited by maximum junction temperature, maximum duty cycle is 0.75.
- $I_{AS} = 3A, L=55mH, V_{DD} = 60V, \text{Starting } T_j = 25^\circ\text{C}.$
- The value of R_{thJA} is measured by placing the device in a still air box which is one cubic foot.



Electrical Characteristics Diagrams

Figure 1. Typ. Output Characteristics

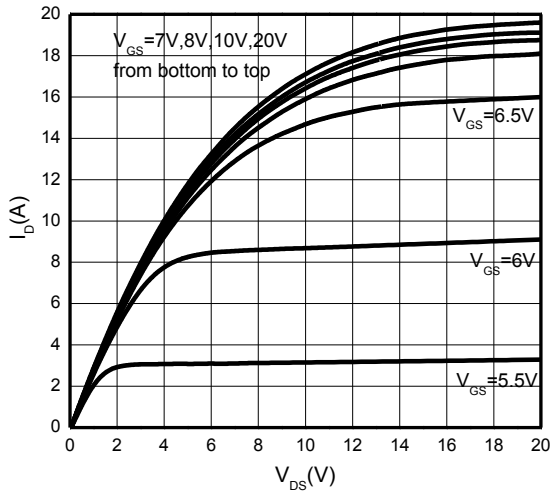


Figure 2. Transfer Characteristics

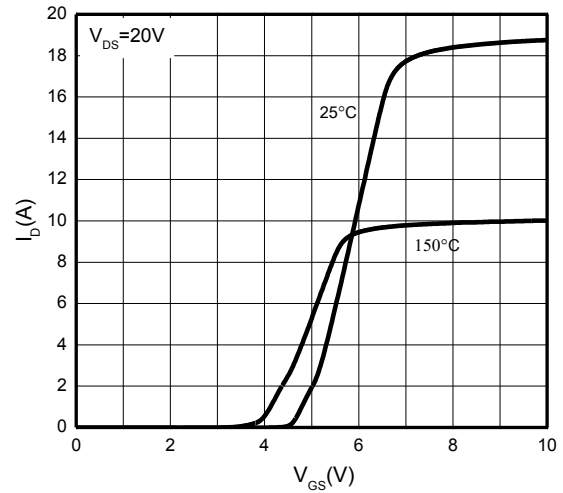


Figure 3. On-Resistance vs. Drain Current

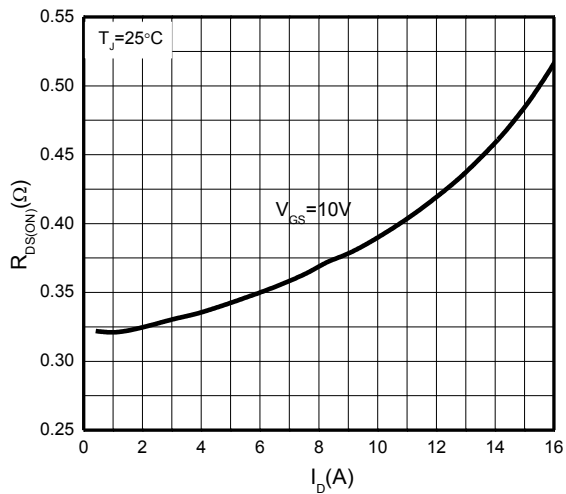


Figure 4. On-Resistance vs. Temperature

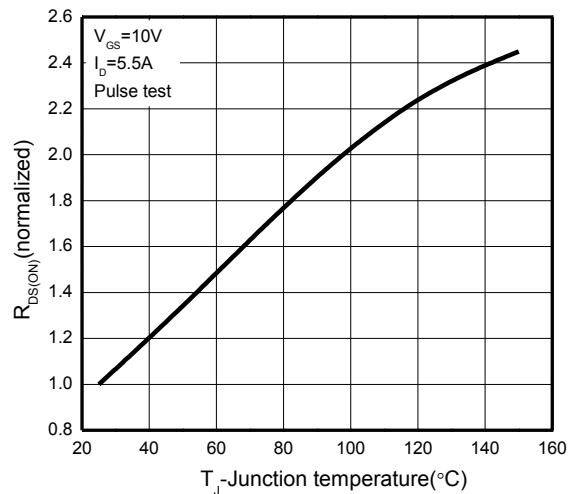


Figure 5. Breakdown Voltage vs. Temperature

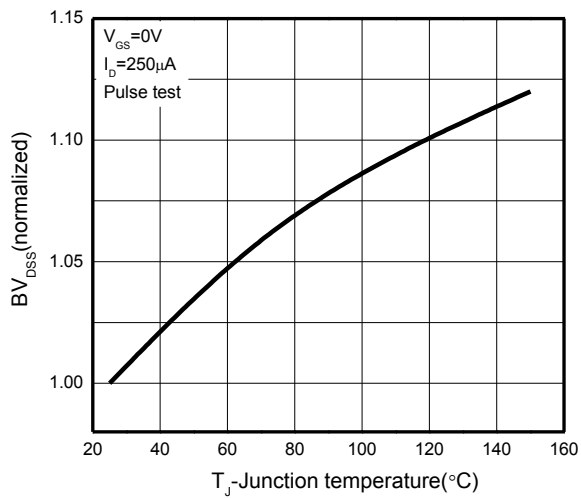


Figure 6. Threshold Voltage vs. Temperature

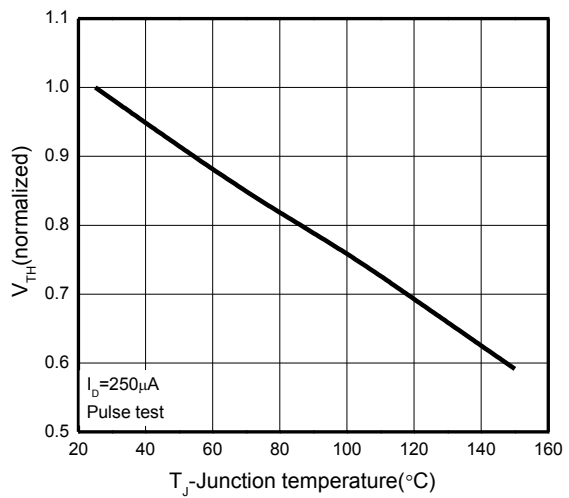




Figure 7. Body-Diode Characteristics

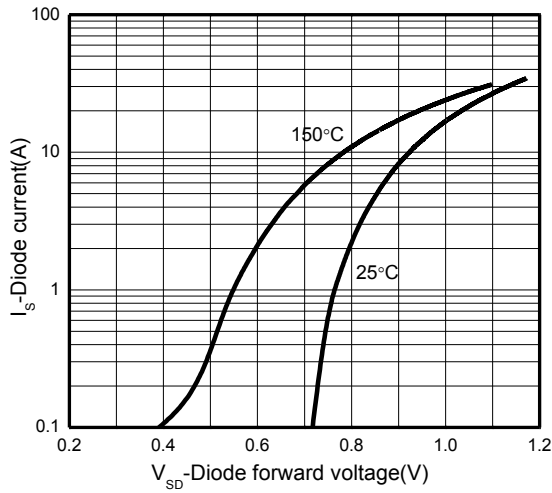


Figure 8. Capacitance Characteristics

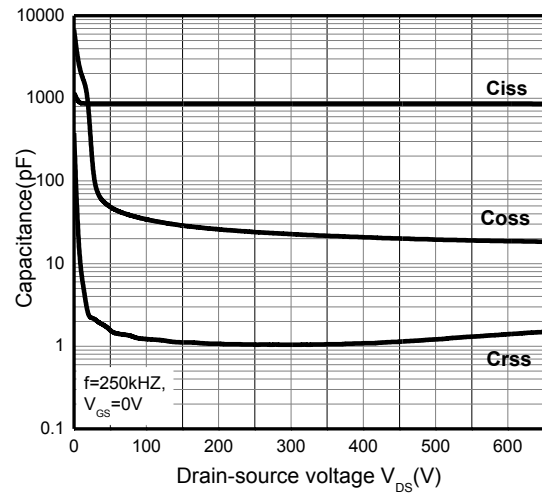


Figure 9. Gate Charge Characteristics

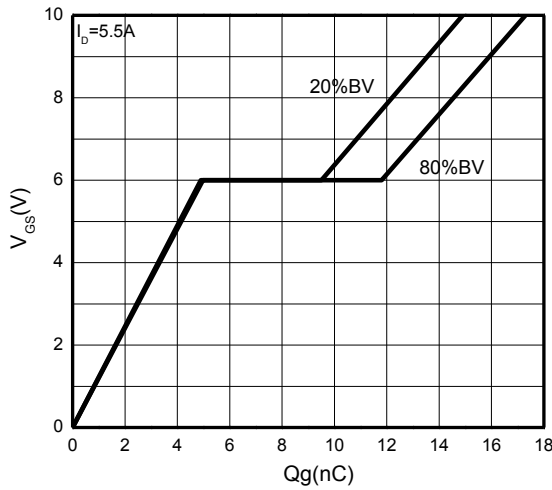


Figure 10. Drain Current Derating

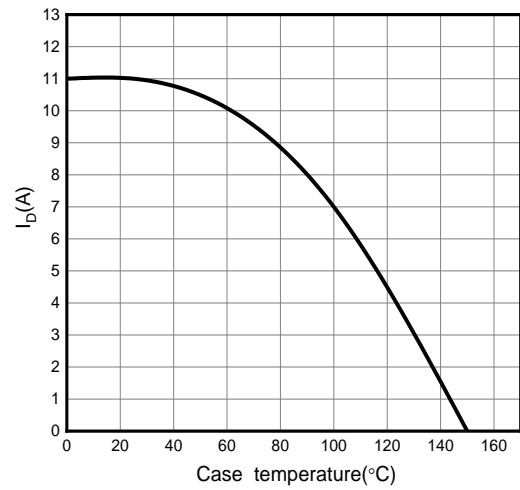


Figure 11. Power Dissipation vs. Temperature

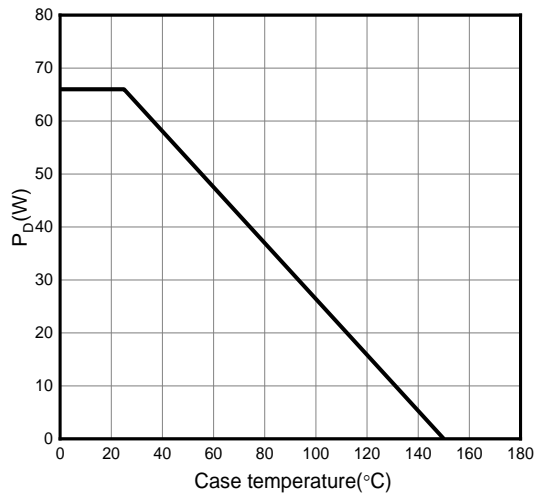


Figure 12. Safe Operating Area

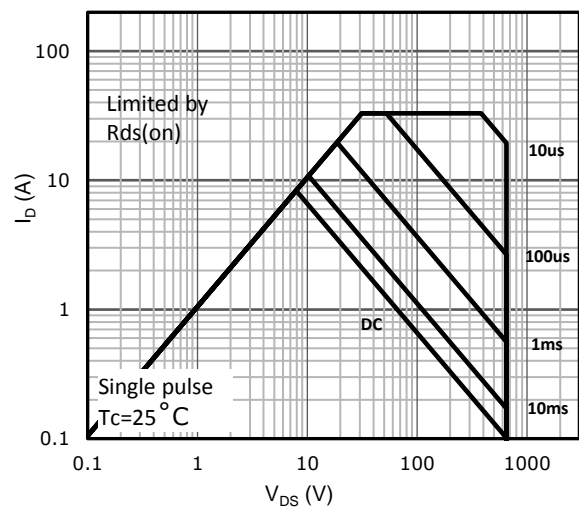
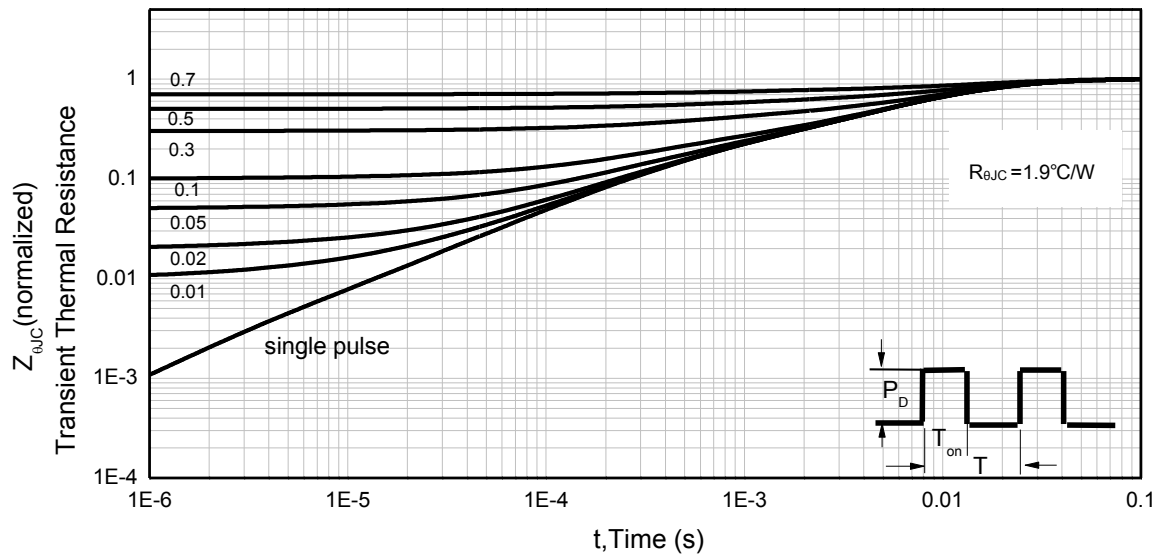




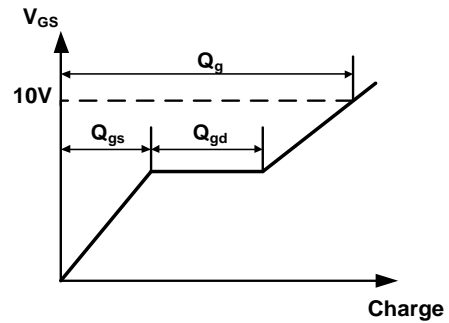
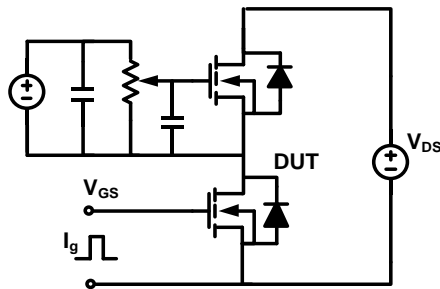
Figure 13. Normalized Maximum Transient Thermal Impedance (R_{thJC})



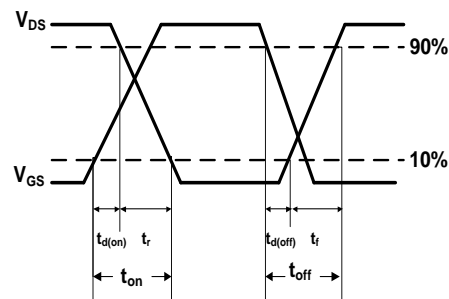
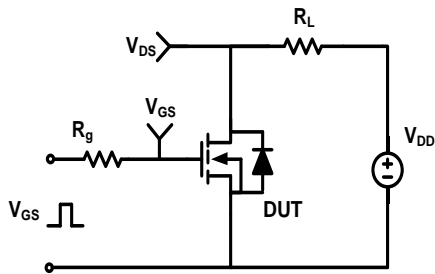


Test Circuit & Waveforms

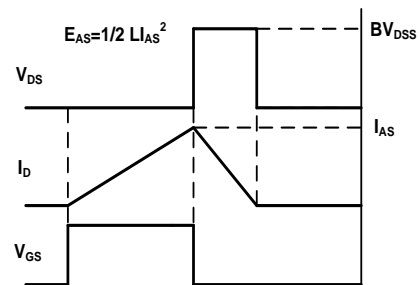
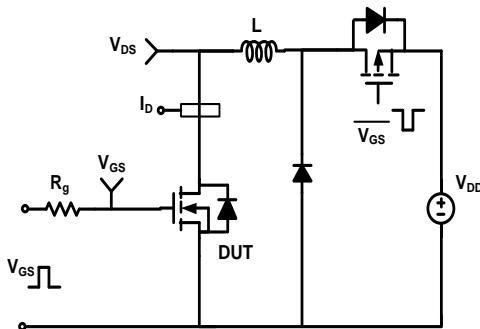
Gate Charge Test Circuit & Waveform



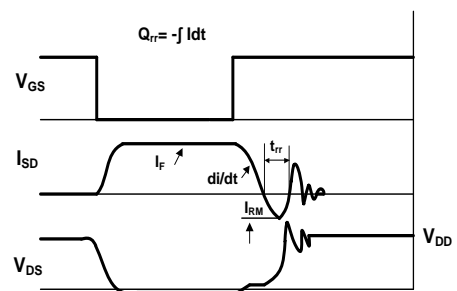
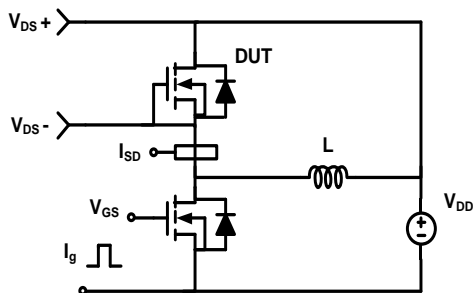
Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveform

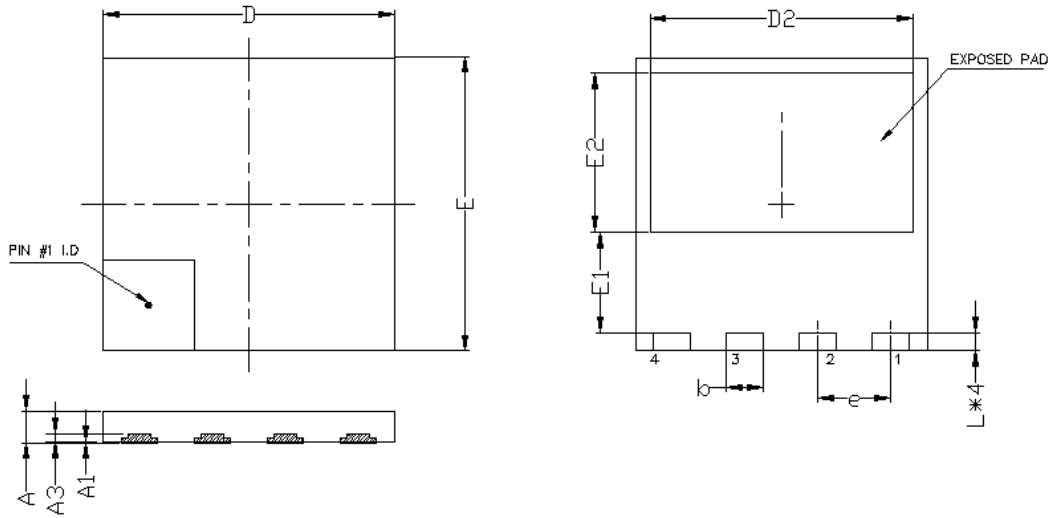


Diode Recovery Test Circuit & Waveform





Mechanical Dimensions for DFN8×8



DIMENSIONS IN MILLIMETERS		
SYMBOL	MIN	MAX
A	0.75	1.00
A1	0.00	0.05
A3	0.10	0.30
b	0.90	1.10
D	7.90	8.10
E	7.90	8.10
D2	7.10	7.30
E1	2.65	2.85
E2	4.25	4.65
e	2.00BSC	
L	0.4	0.6



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