

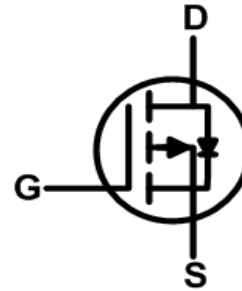


- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

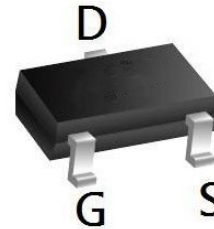
### Description

The WL30P10L is the highest performance trench P-ch MOSFETs with extreme high cell density, which provide excellent R<sub>DS(on)</sub> and gate charge for most of the synchronous buck converter applications .

The WL30P10L meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.



### SOT23-3L Pin Configuration



### Product Summary

BVDSS	R <sub>DS(on)</sub>	I <sub>D</sub>
-30V	14mΩ	-9.5A

### Absolute Maximum Ratings (T<sub>A</sub>=25°C unless otherwise specified)

Symbol	Parameter	Max.	Units
V <sub>DSS</sub>	Drain-Source Voltage	-30	V
V <sub>GSS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Continuous Drain Current	T <sub>A</sub> = 25°C	-9.5
		T <sub>A</sub> = 100°C	-5.5
I <sub>DM</sub>	Pulsed Drain Current <sup>note1</sup>	-46	A
E <sub>AS</sub>	Single Pulsed Avalanche Energy <sup>note2</sup>	35	mJ
P <sub>D</sub>	Power Dissipation	T <sub>A</sub> = 25°C	3.0
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient	48	°C/W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C



**Electrical Characteristics** ( $T_J=25^{\circ}\text{C}$  unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D = -250\mu A$	-30	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -30V, V_{GS}=0V,$	-	-	-1	$\mu A$
$I_{GSS}$	Gate to Body Leakage Current	$V_{DS}=0V, V_{GS} = \pm 20V$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D = -250\mu A$	-1.0	-1.6	-2.5	V
$R_{DS(on)}$	Static Drain-Source on-Resistance <small>Note3</small>	$V_{GS} = -10V, I_D = -5A$	-	14	20	m $\Omega$
		$V_{GS} = -4.5V, I_D = -5A$	-	19	27	
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = -15V, V_{GS}=0V,$ $f=1.0MHz$	-	1330	-	pF
$C_{oss}$	Output Capacitance		-	183	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	156	-	pF
$Q_g$	Total Gate Charge	$V_{DS} = -15V, I_D = -5A,$ $V_{GS} = -10V$	-	22	-	nC
$Q_{gs}$	Gate-Source Charge		-	1.0	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge		-	1.8	-	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = -15V, I_D = -10A,$ $V_{GS} = -10V, R_{GEN} = 2.5\Omega$	-	9	-	ns
$t_r$	Turn-on Rise Time		-	13	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	48	-	ns
$t_f$	Turn-off Fall Time		-	20	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain to Source Diode Forward Current		-	-	-9.5	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-46	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS}=0V, I_S = -15A$	-	-0.8	-1.2	V
$t_{rr}$	Reverse Recovery Time	$T_J=25^{\circ}\text{C},$	-	64	-	ns
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = -24V, I_F = -2.8A,$ $di/dt = -100A/\mu s$	-	25	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition:  $T_J=25^{\circ}\text{C}, V_{GS}=10V, R_G=25\Omega, L=0.5mH, I_{AS}=-12.7A$

3. Pulse Test: Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 0.5\%$



### Typical Performance Characteristics

Figure 1: Output Characteristics

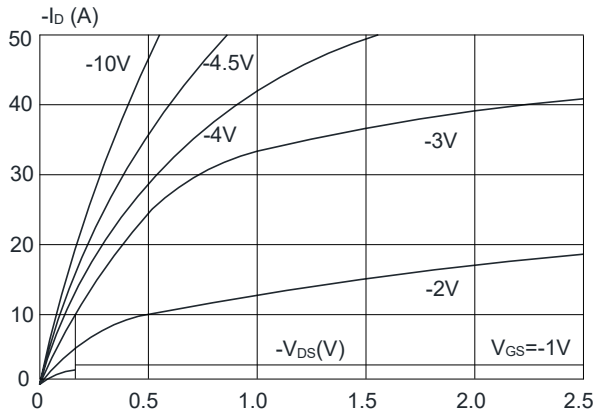


Figure 2: Typical Transfer Characteristics

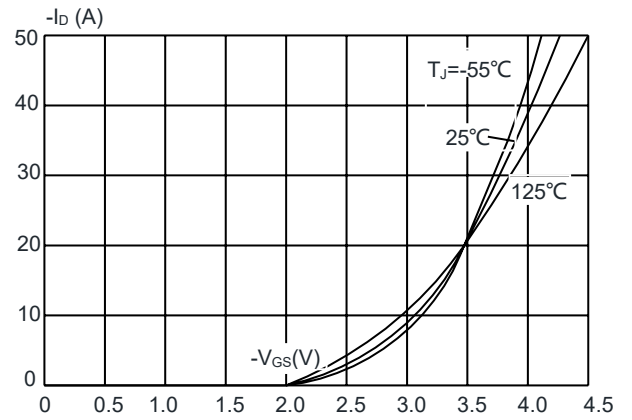


Figure 3: On-resistance vs. Drain Current

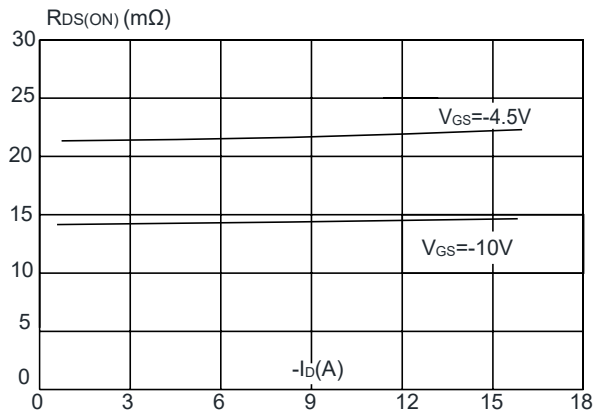


Figure 4: Body Diode Characteristics

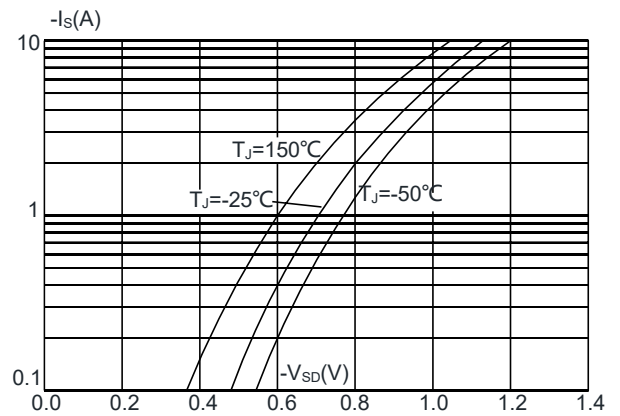


Figure 5: Gate Charge Characteristics

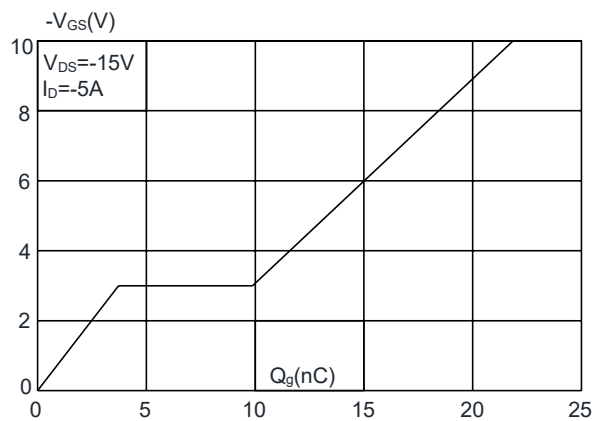
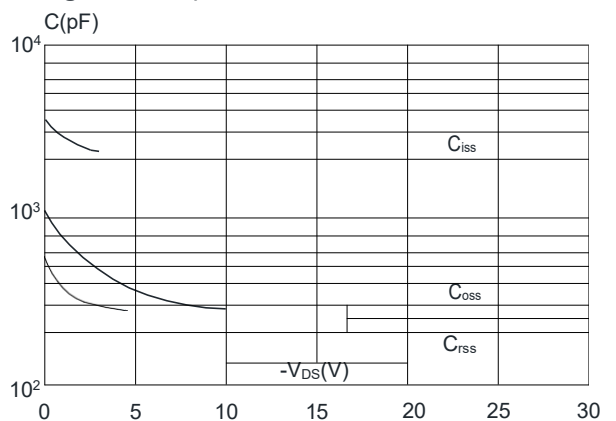


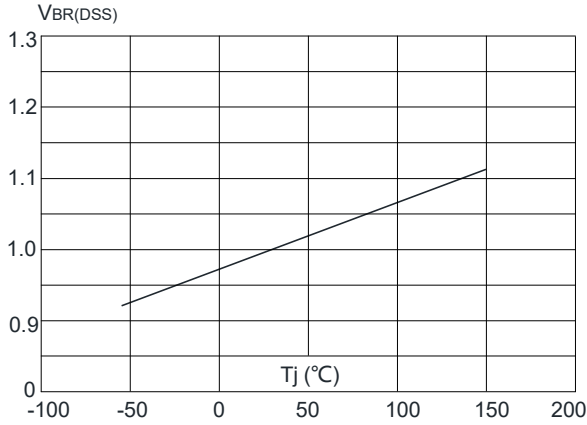
Figure 6: Capacitance Characteristics



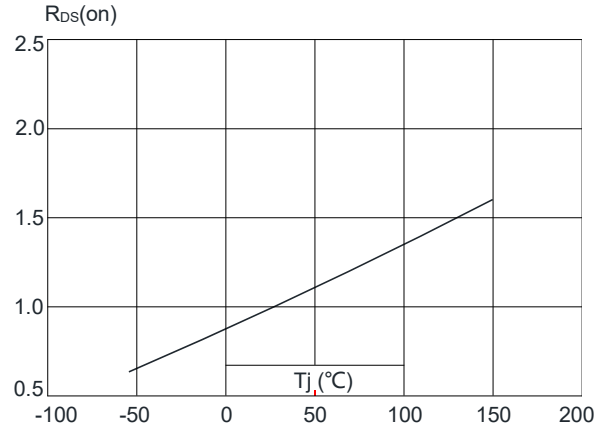


P-Ch 30V Fast Switching MOSFETs

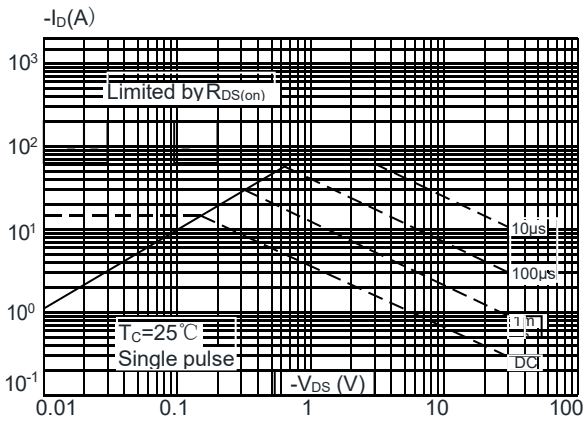
**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature



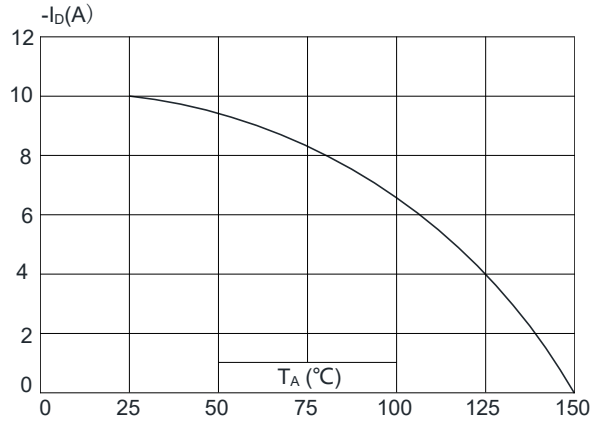
**Figure 8:** Normalized on Resistance vs. Junction Temperature



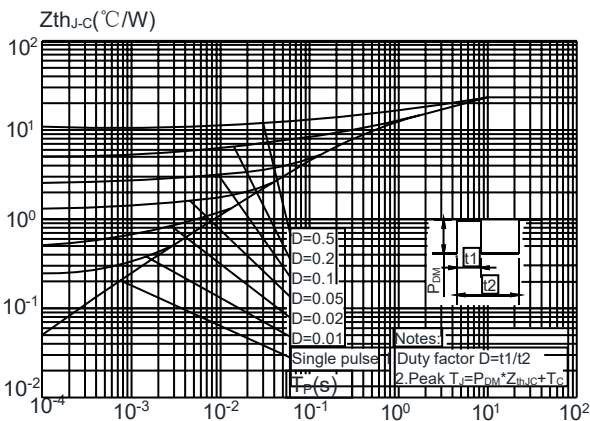
**Figure 9:** Maximum Safe Operating Area



**Figure 10:** Maximum Continuous Drain Current vs. Ambient Temperature



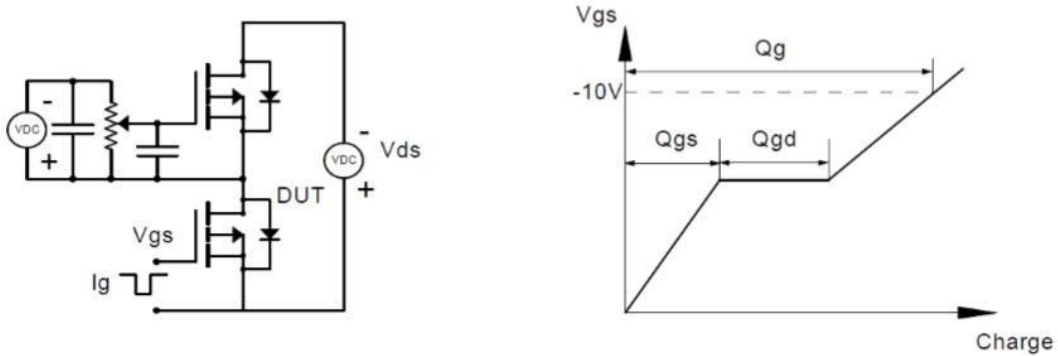
**Figure 11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case



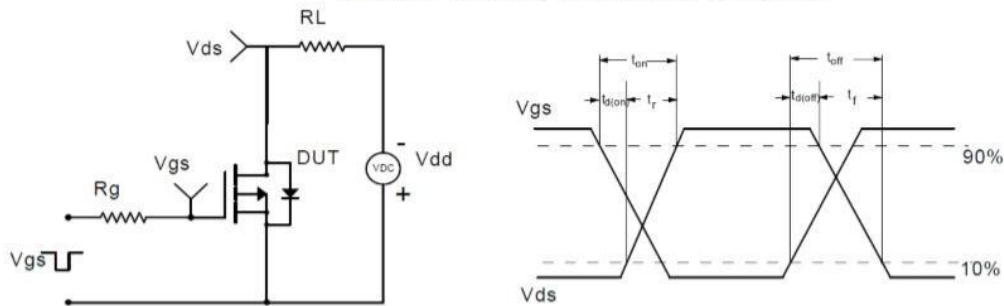


### Test Circuit

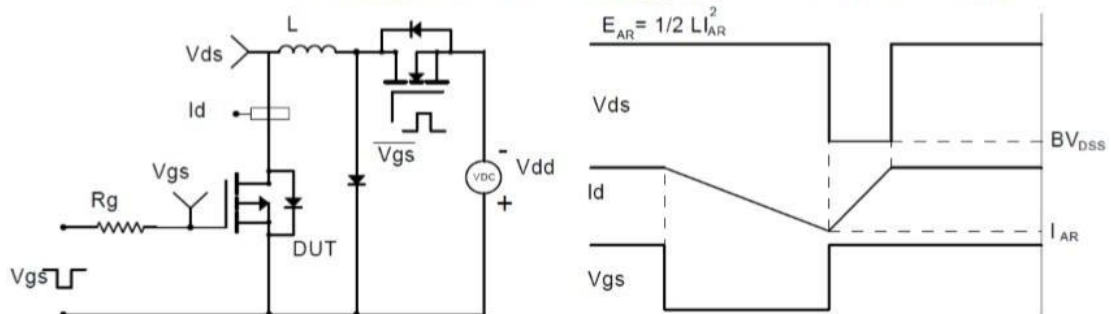
Gate Charge Test Circuit & Waveform



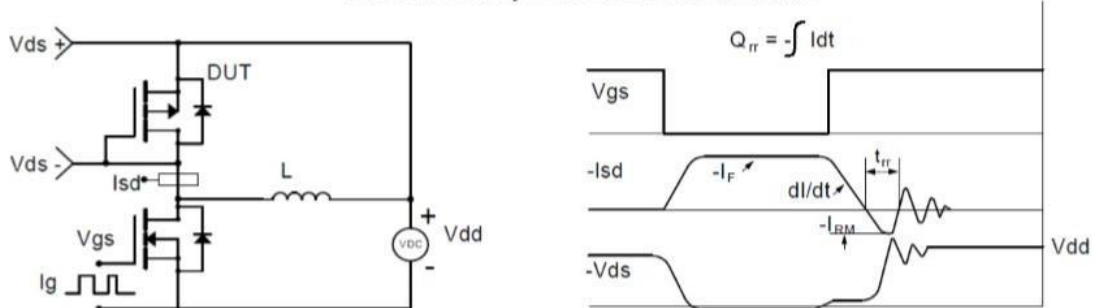
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

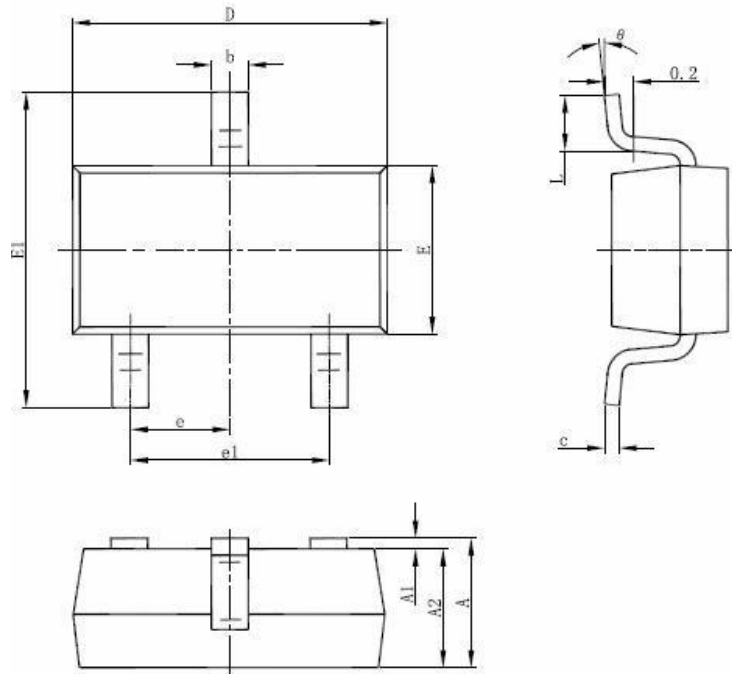


Diode Recovery Test Circuit & Waveforms





SOT-23-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
$\theta$	0°	8°	0°	8°



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