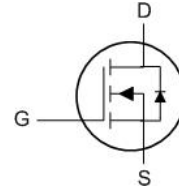




- ★ Super Low Gate Charge
- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

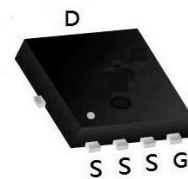


Description

The WLQ100N03F is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The WLQ100N03F meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

PDFN5060-8L Pin Configuration



Product Summary

BVDSS	RDSON	ID
30V	3.5mΩ	100A

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		10s	Steady State	
V_{DS}	Drain-Source Voltage	30		V
V_{GS}	Gate-Source Voltage	±20		V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS}@ 10V^1$	100		A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS}@ 10V^1$	50		A
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS}@ 10V^1$	30	19	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS}@ 10V^1$	25	16	A
I_{DM}	Pulsed Drain Current ²	162		A
EAS	Single Pulse Avalanche Energy ³	144.7		mJ
I_{AS}	Avalanche Current	53.8		A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	62.5		W
$P_D@T_A=25^\circ C$	Total Power Dissipation ⁴	6	2.42	W
T_{STG}	Storage Temperature Range	-55 to 175		°C
T_J	Operating Junction Temperature Range	-55 to 175		°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	62	°C/W
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹ (t ≤ 10s)	---	25	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	2.4	°C/W



Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 30V, V _{GS} = 0V,	-	-	1.0	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1.0	1.5	2.5	V
R _{DS(on)}	Static Drain-Source on-Resistance <small>note3</small>	V _{GS} = 10V, I _D = 30A	-	3.5	4.7	mΩ
		V _{GS} = 4.5V, I _D = 20A	-	7.0	10	
C _{iss}	Input Capacitance	V _{DS} = 15V, V _{GS} = 0V, f = 1.0MHz	-	2100	-	pF
C _{oss}	Output Capacitance		-	326	-	pF
C _{rss}	Reverse Transfer Capacitance		-	282	-	pF
Q _g	Total Gate Charge	V _{DS} = 15V, I _D = 30A, V _{GS} = 10V	-	45	-	nC
Q _{gs}	Gate-Source Charge		-	3	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	15	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} = 15V, I _D = 30A, R _{GEN} = 3Ω, V _{GS} = 10V	-	21	-	ns
t _r	Turn-on Rise Time		-	32	-	ns
t _{d(off)}	Turn-off Delay Time		-	59	-	ns
t _f	Turn-off Fall Time		-	34	-	ns
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	50	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	200	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _S = 30A	-	-	1.2	V
t _{rr}	Body Diode Reverse Recovery Time	I _F = 20A, dI/dt = 100A/μs	-	15	-	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	4	-	nC

Notes: 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: T_J = 25°C, V_G = 10V, R_G = 25Ω, L = 0.5mH, I_{AS} = 18.4A

3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 0.5%



Figure 1: Output Characteristics

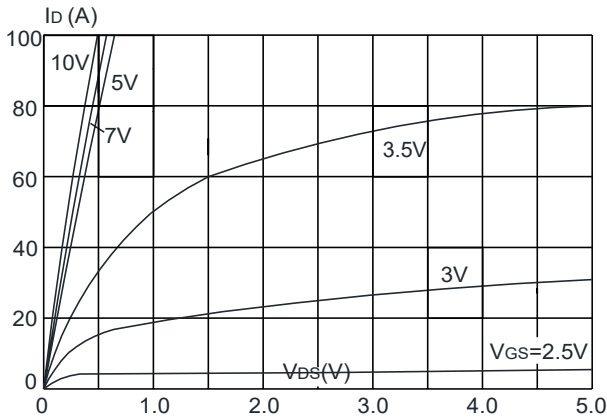


Figure 2: Typical Transfer Characteristics

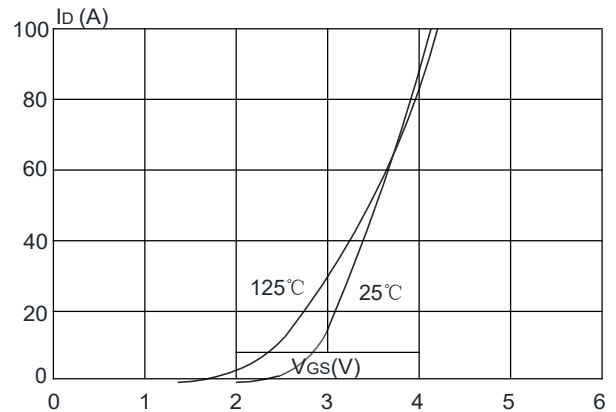


Figure 3: On-resistance vs. Drain Current

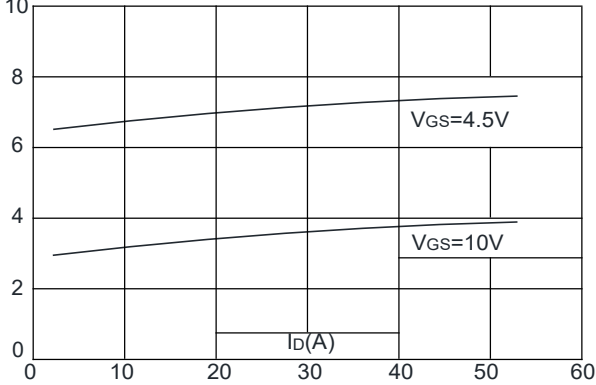


Figure 4: Body Diode Characteristics

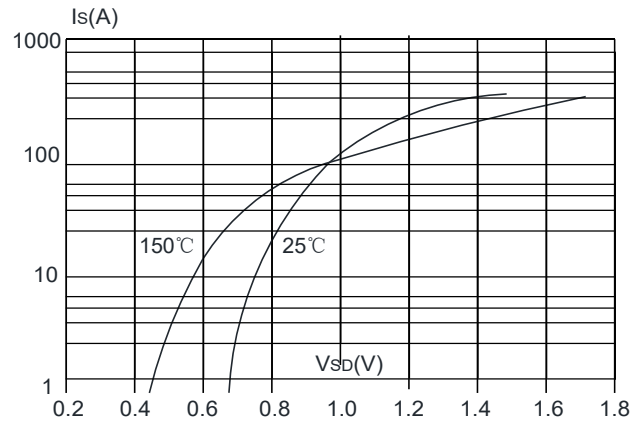


Figure 5: Gate Charge Characteristics

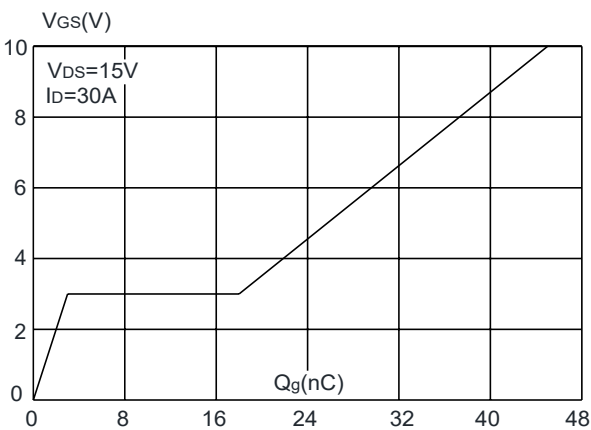


Figure 6: Capacitance Characteristics

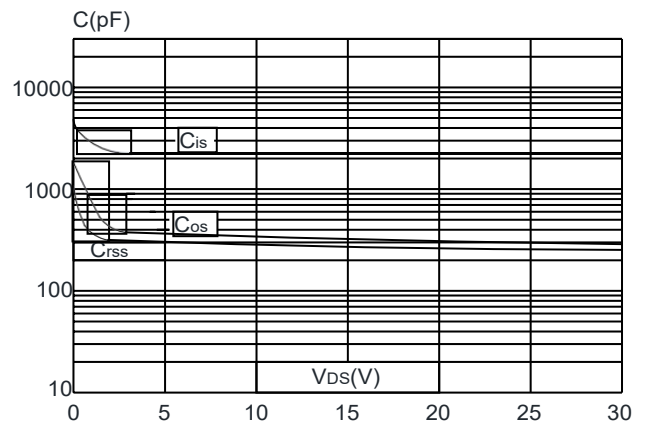




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

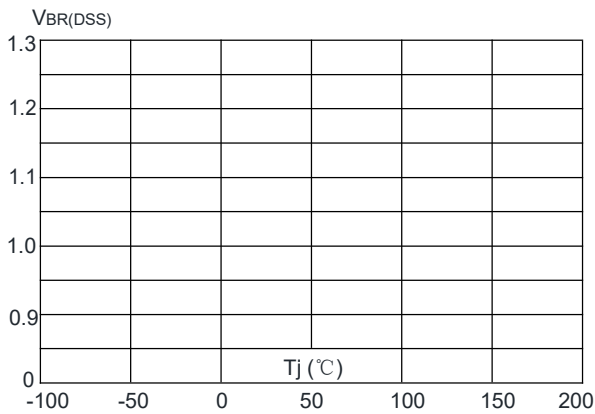


Figure 8: Normalized on Resistance vs. Junction Temperature

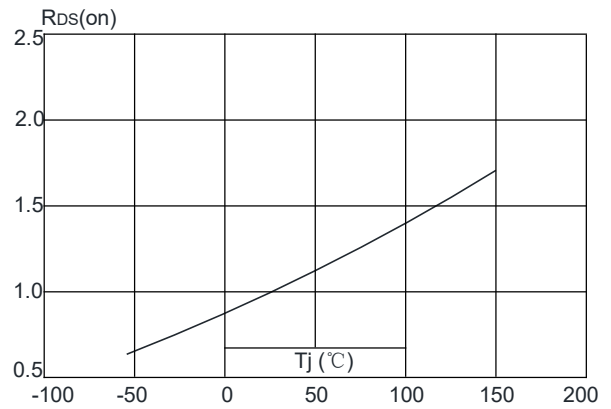


Figure 9: Maximum Safe Operating Area

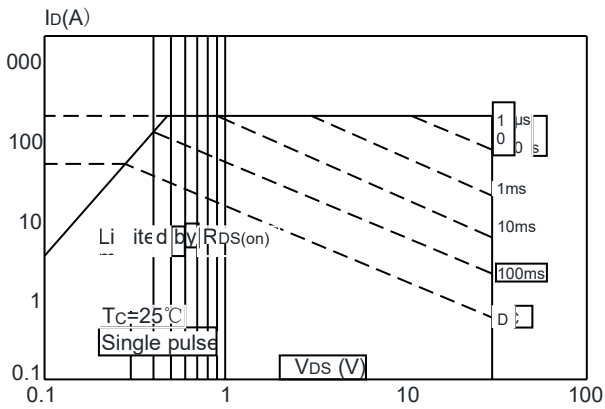


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

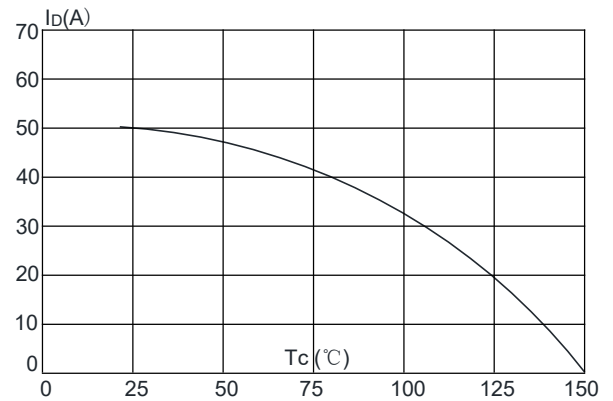
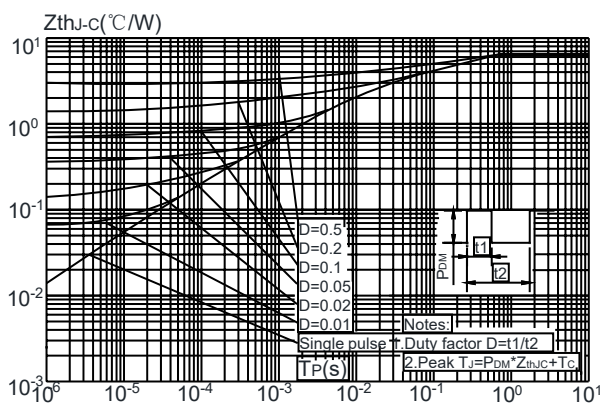


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case (PDFN3.3*3.3-8L)





Test Circuit

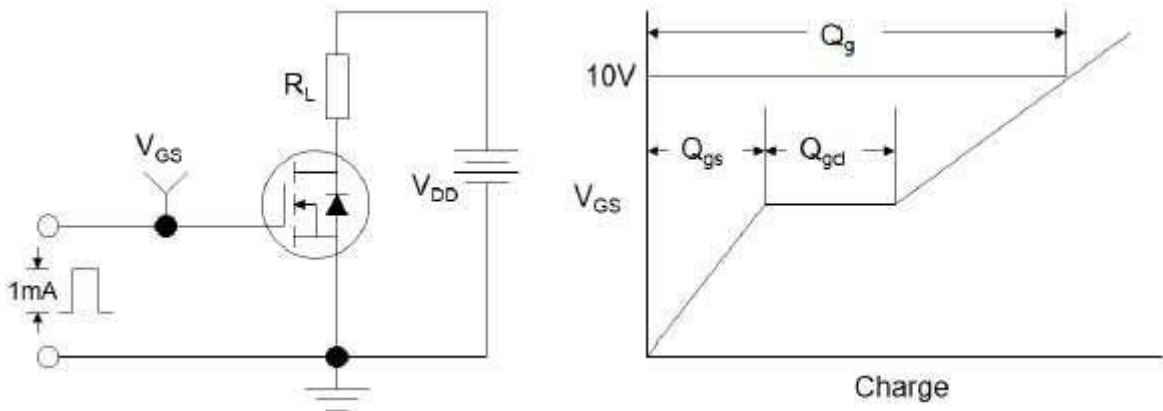


Figure1:Gate Charge Test Circuit & Waveform

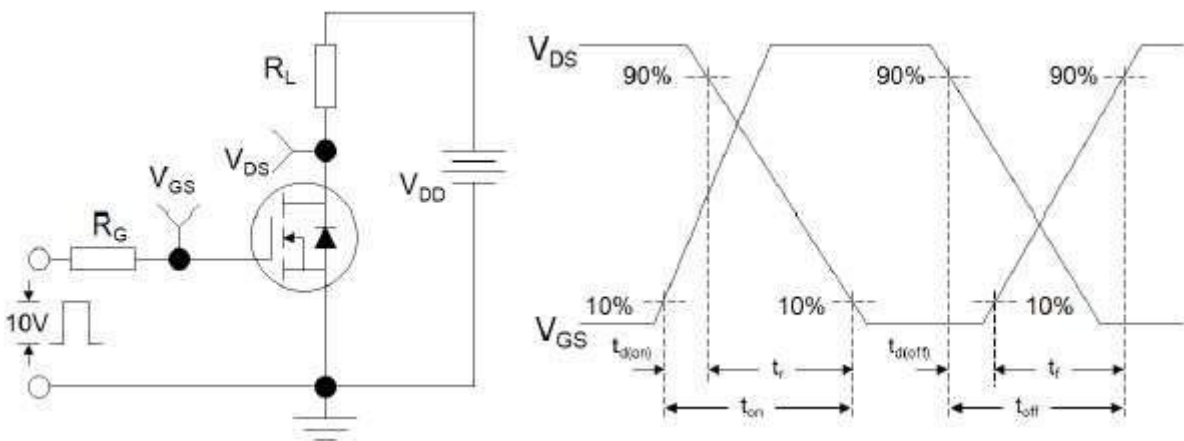


Figure 2: Resistive Switching Test Circuit & Waveforms

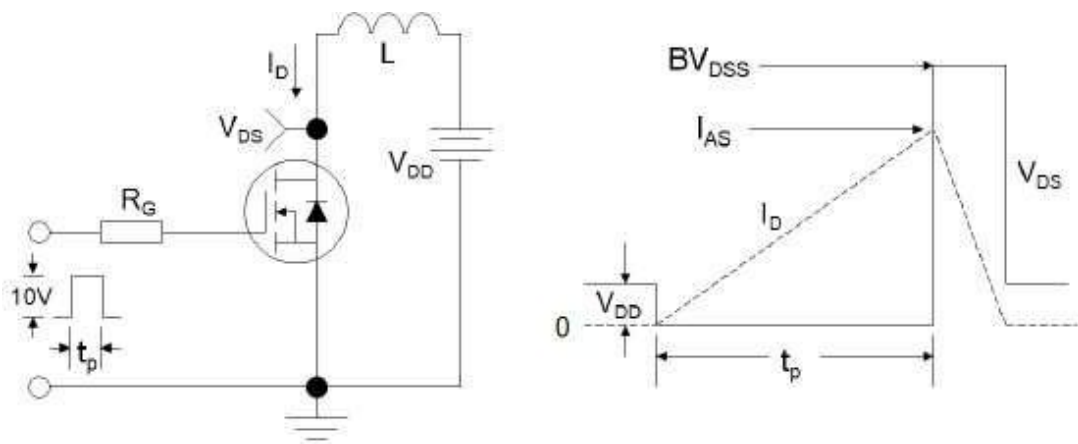
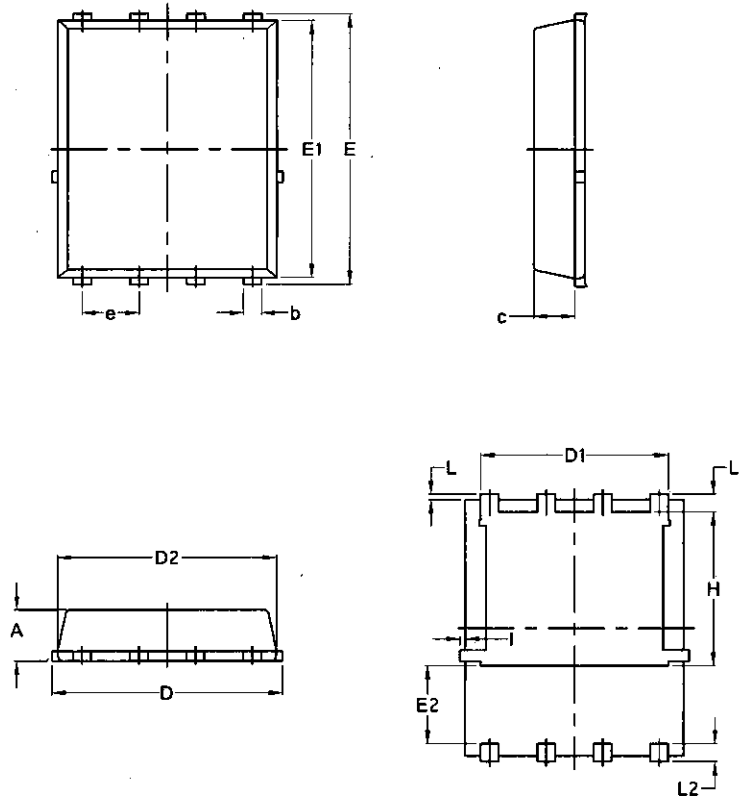


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



Package Mechanical Data-DFN5060-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070



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