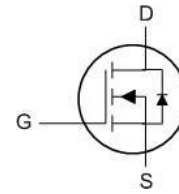




### Features

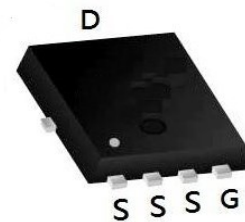
- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$



### Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

### PDFN5060-8L Pin Configuration



### Product Summary

BVDSS	RDSON	ID
100V	12mΩ	50A

### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		$V_{DS}$	100	V
Gate-Source Voltage		$V_{GS}$	±20	V
Continuous Drain Current	$T_C=25^\circ\text{C}$	$I_D$	50	A
	$T_C=100^\circ\text{C}$		29	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	184	A
Single Pulse Avalanche Energy <sup>2</sup>		<b>EAS</b>	80	mJ
Total Power Dissipation	$T_C=25^\circ\text{C}$	$P_D$	71.4	W
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 to 150	°C

### Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient <sup>3</sup>	$R_{\theta JA}$	52	°C/W
Thermal Resistance from Junction-to-Lead	$R_{\theta JC}$	1.75	°C/W



### Electrical Characteristics ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Characteristics</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100	-	-	V
Gate-Body Leakage Current	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$T_J = 25^\circ\text{C}$	$V_{DS} = 100V, V_{GS} = 0V$	-	-	1	$\mu A$
	$T_J = 100^\circ\text{C}$		-	-	100	
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.7	2.5	V
Drain-Source on-Resistance <sup>4</sup>	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$	-	12	17	m $\Omega$
		$V_{GS} = 4.5V, I_D = 10A$	-	14.5	20	
Forward Transconductance <sup>4</sup>	$g_{fs}$	$V_{DS} = 10V, I_D = 20A$	-	54	-	S
<b>Dynamic Characteristics<sup>5</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 50V, V_{GS} = 0V, f = 1\text{MHz}$	-	1208	-	pF
Output Capacitance	$C_{oss}$		-	144	-	
Reverse Transfer Capacitance	$C_{rss}$		-	11.3	-	
Gate Resistance	$R_G$	$f = 1\text{MHz}$	-	1.8	-	$\Omega$
<b>Switching Characteristics<sup>5</sup></b>						
Total Gate Charge	$Q_g$	$V_{GS} = 10V, V_{DS} = 50V, I_D = 20A$	-	22.7	-	nC
Gate-Source Charge	$Q_{gs}$		-	3	-	
Gate-Drain Charge	$Q_{gd}$		-	5	-	
Turn-on Delay Time	$t_{d(on)}$	$V_{GS} = 10V, V_{DD} = 50V, R_G = 3\Omega, I_D = 20A$	-	9.2	-	ns
Rise Time	$t_r$		-	3.6	-	
Turn-off Delay Time	$t_{d(off)}$		-	25.6	-	
Fall Time	$t_f$		-	4.4	-	
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 20A, di/dt = 100A/\mu s$	-	30	-	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	42	-	nC
<b>Drain-Source Body Diode Characteristics</b>						
Diode Forward Voltage <sup>4</sup>	$V_{SD}$	$I_S = 20A, V_{GS} = 0V$	-	-	1.2	V
Continuous Source Current	$T_C = 25^\circ\text{C}$	$I_S$	-	-	50	A

1. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)} = 150^\circ\text{C}$

2. The EAS data shows Max. rating . The test condition is  $V_{DD} = 25V, V_{GS} = 10V, L = 0.1\text{mH}, I_{AS} = 40A$ .

3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.

4. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$ .

5. This value is guaranteed by design hence it is not included in the production test.



### Typical Characteristics

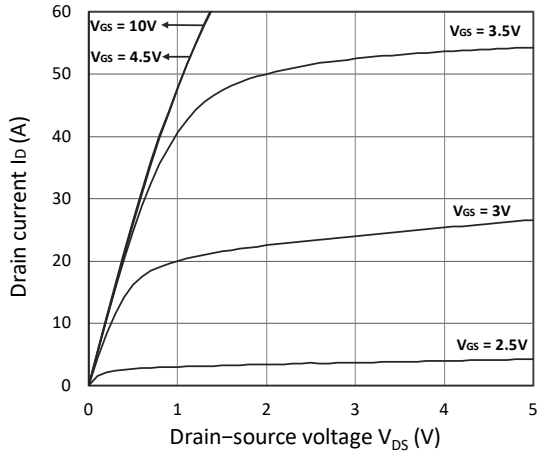


Figure 1. Output Characteristics

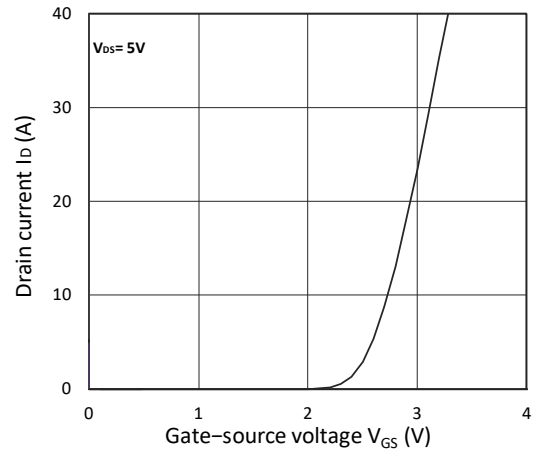


Figure 2. Transfer Characteristics

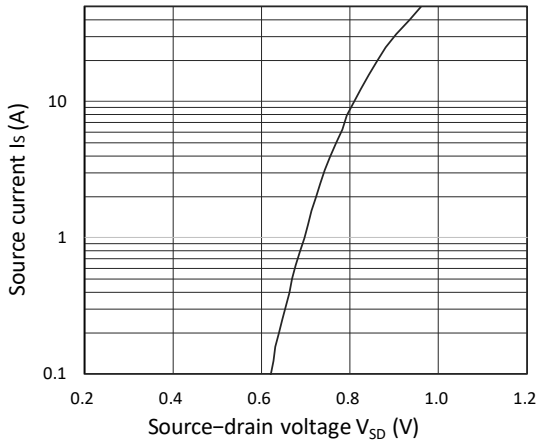


Figure 3. Forward Characteristics of Reverse

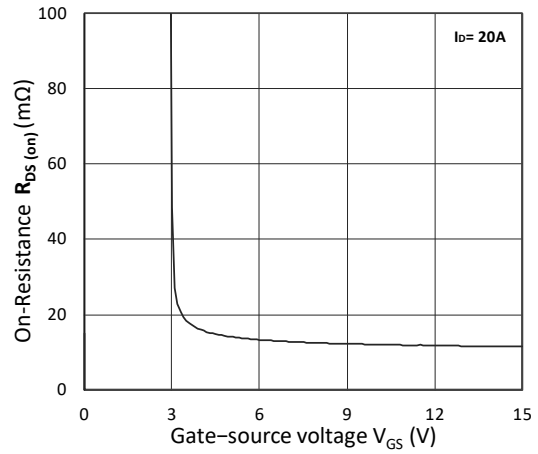


Figure 4.  $R_{DS(ON)}$  vs.  $V_{GS}$

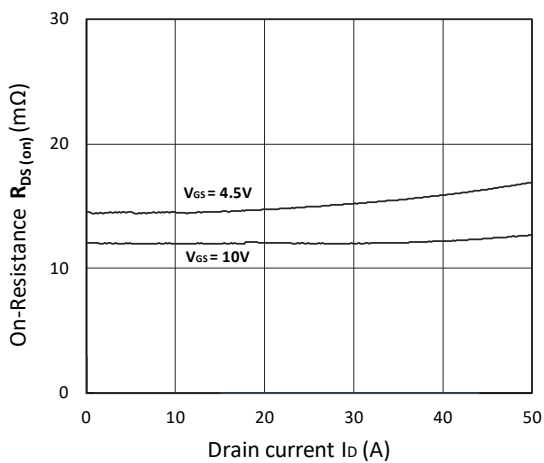


Figure 5.  $R_{DS(ON)}$  vs.  $I_D$

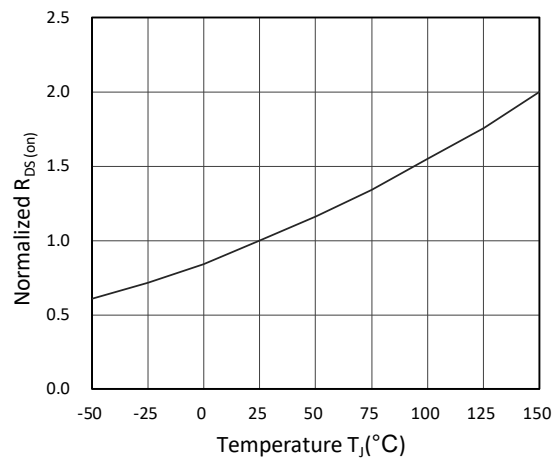


Figure 6. Normalized  $R_{DS(ON)}$  vs. Temperature

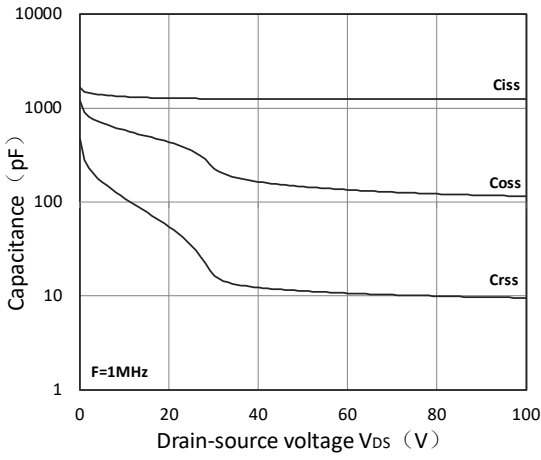


Figure 7. Capacitance Characteristics

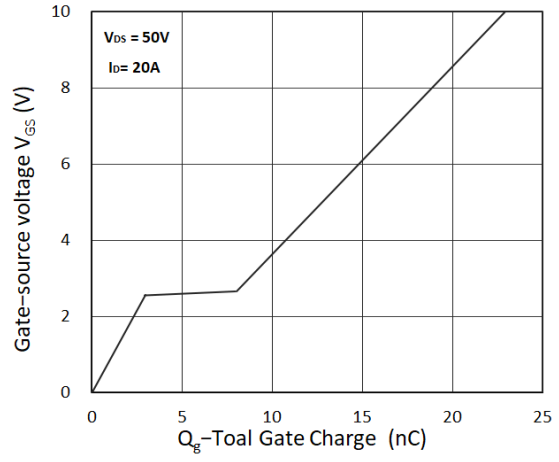


Figure 8. Gate Charge Characteristics

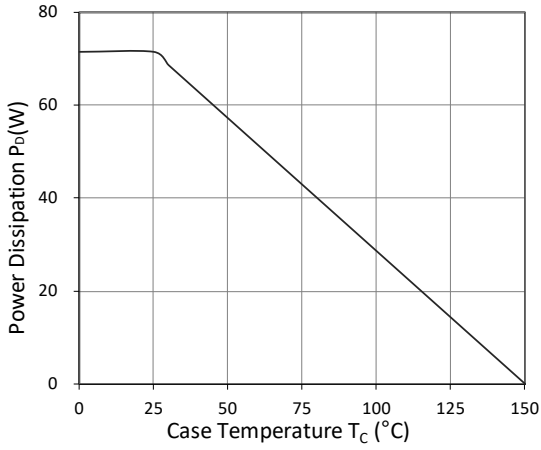


Figure 9. Power Dissipation

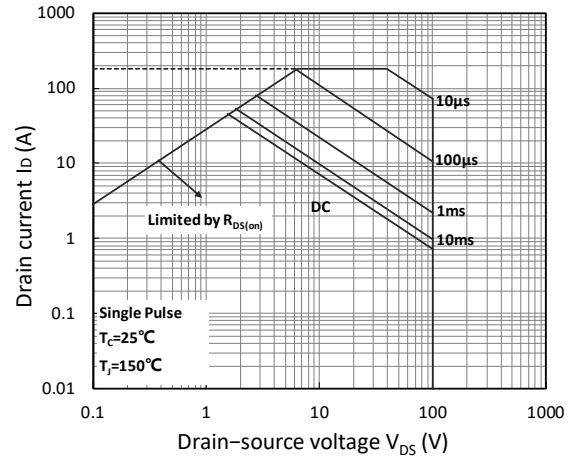


Figure 10. Safe Operating Area

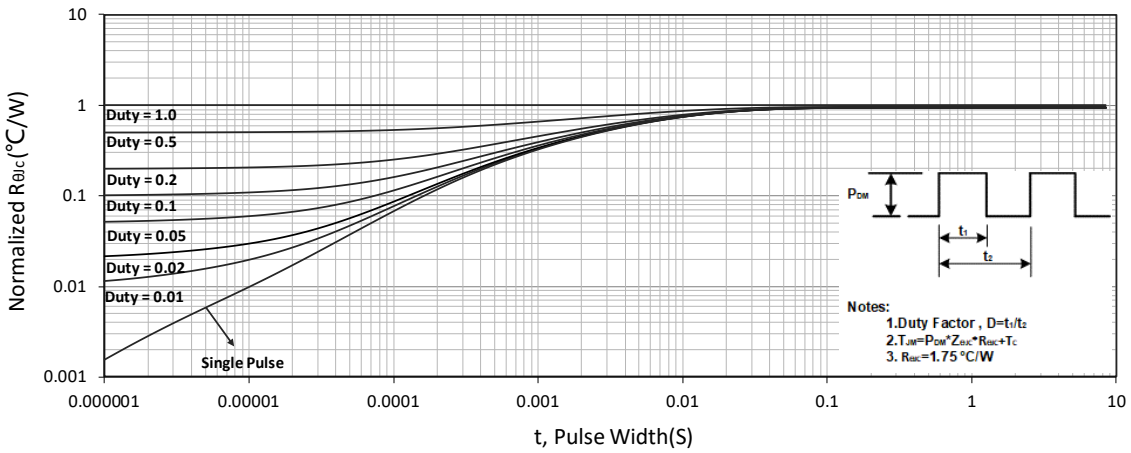


Figure 11. Normalized Maximum Transient Thermal Impedance



### Test Circuit

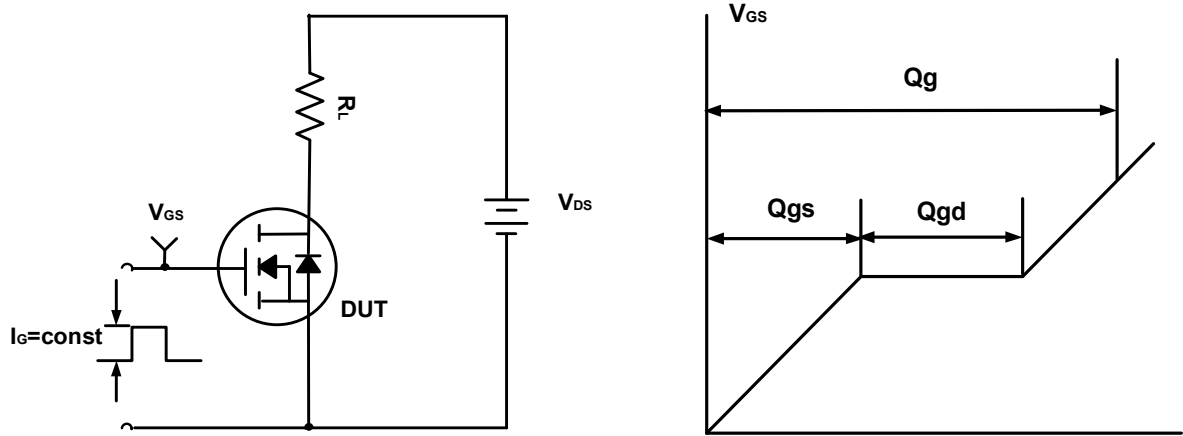


Figure A. Gate Charge Test Circuit & Waveforms

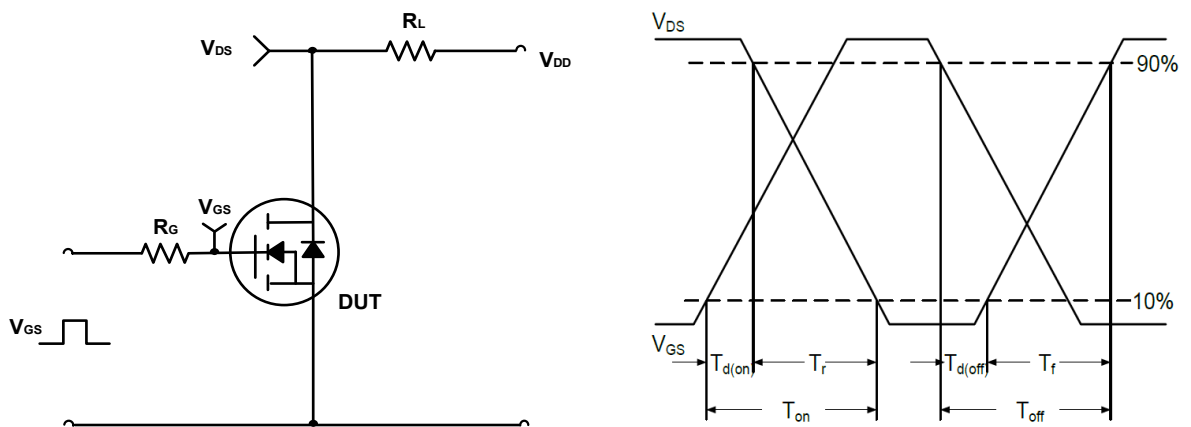


Figure B. Switching Test Circuit & Waveforms

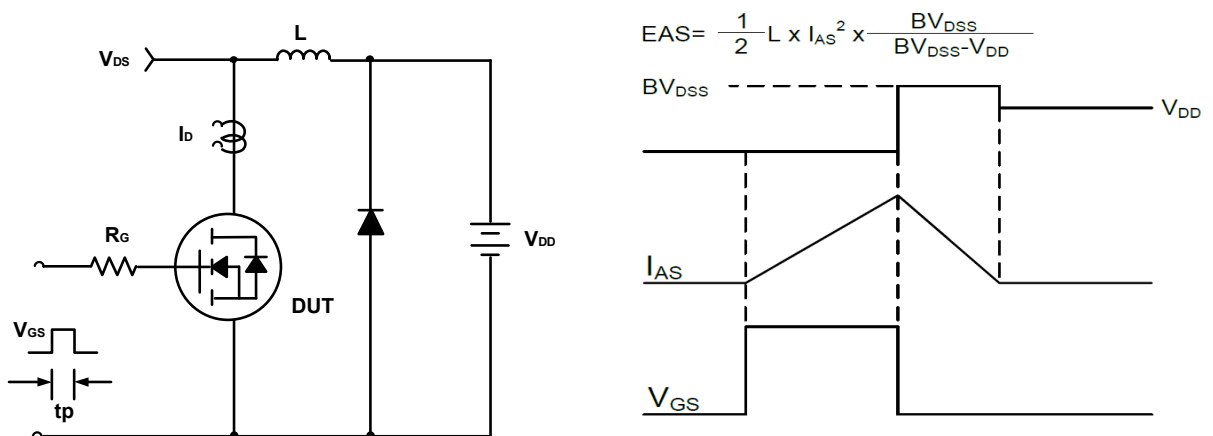
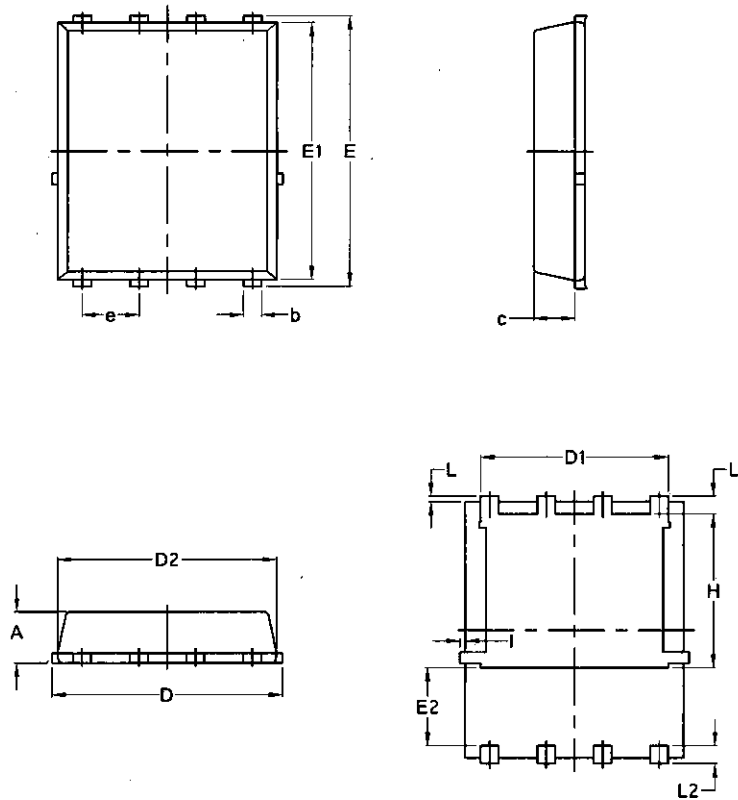


Figure C. Unclamped Inductive Switching Circuit & Waveforms



Package Mechanical Data-PDFN5060-8L-Single



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070



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