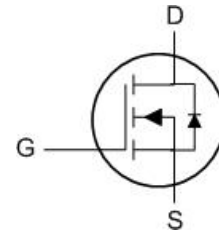




### Features

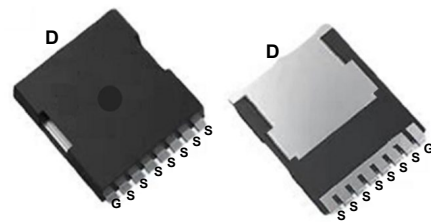
- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$



### Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

### TOLL-8L Pin Configuration



### Product Summary

BVDSS	RDSON	ID
60V	1.25mΩ	400A

### Absolute Maximum Ratings (TA = 25°C, unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	±20	V
Continuous Drain Current	$I_D$	$T_C=25^\circ\text{C}$	400
		$T_C=100^\circ\text{C}$	268
Pulsed Drain Current <sup>1</sup>	$I_{DM}$	1512	A
Single Pulse Avalanche Energy <sup>2</sup>	<b>EAS</b>	500	mJ
Total Power Dissipation	$P_D$	454.5	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	°C

### Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient <sup>3</sup>	$R_{\theta JA}$	39	°C/W
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	0.33	°C/W



### Electrical Characteristics (T<sub>J</sub> = 25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Characteristics</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	60	-	-	V
Gate-body Leakage current	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T <sub>J</sub> =25°C	V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V	-	-	1	μA
	T <sub>J</sub> =100°C		-	-	100	
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2	2.9	4	V
Drain-Source on-Resistance <sup>4</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A	-	1.25	1.55	mΩ
Forward Transconductance <sup>4</sup>	g <sub>fs</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =20A	-	62	-	S
<b>Dynamic Characteristics<sup>5</sup></b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V, f = 1MHz	-	5990	-	pF
Output Capacitance	C <sub>oss</sub>		-	2257	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	86	-	
Gate Resistance	R <sub>g</sub>	f = 1MHz	-	2.6	-	Ω
<b>Switching Characteristics<sup>5</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 30V, I <sub>D</sub> =20A	-	102	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	24.6	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	28.2	-	
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 10V, V <sub>DD</sub> = 30V, R <sub>G</sub> = 3Ω, I <sub>D</sub> = 20A	-	15.6	-	ns
Rise Time	t <sub>r</sub>		-	29	-	
Turn-off Delay Time	t <sub>d(off)</sub>		-	63	-	
Fall Time	t <sub>f</sub>		-	51	-	
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 20A, dI/dt=100A/μs	-	80	-	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>		-	114	-	nC
<b>Drain-Source Body Diode Characteristics</b>						
Diode Forward Voltage <sup>4</sup>	V <sub>SD</sub>	I <sub>S</sub> = 20A, V <sub>GS</sub> = 0V	-	-	1.2	V
Continuous Source Current	I <sub>S</sub>	T <sub>C</sub> =25°C	-	-	400	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C.
2. The test condition is V<sub>DD</sub>= 90V, V<sub>GS</sub>= 10V, L= 0.4mH, I<sub>AS</sub>= 50A.
3. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.



### Typical Characteristics

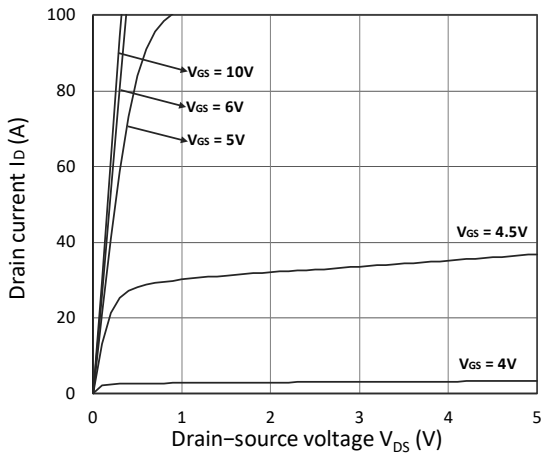


Figure 1. Output Characteristics

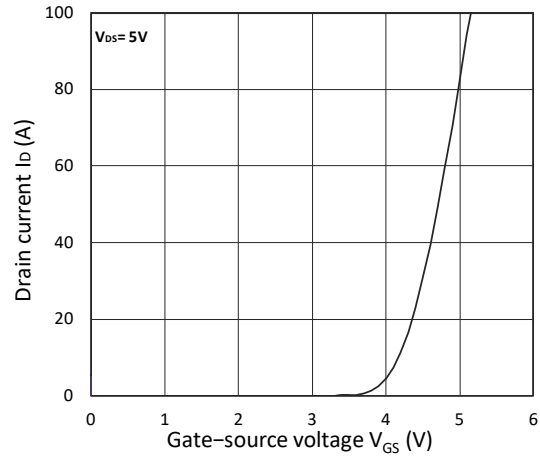


Figure 2. Transfer Characteristics

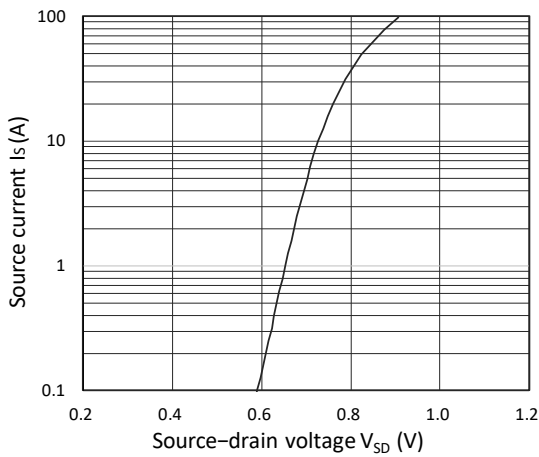


Figure 3. Forward Characteristics of Reverse

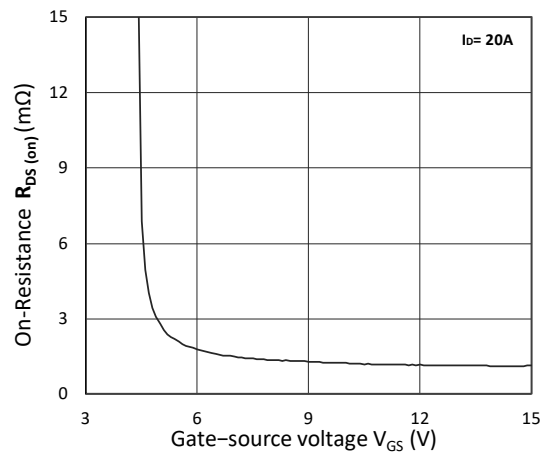


Figure 4.  $R_{DS(on)}$  vs.  $V_{GS}$

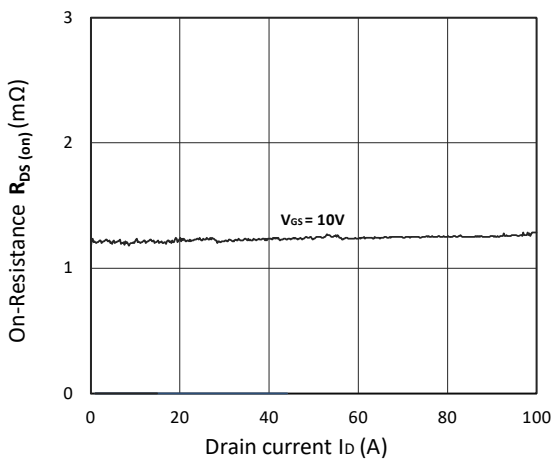


Figure 5.  $R_{DS(on)}$  vs.  $I_D$

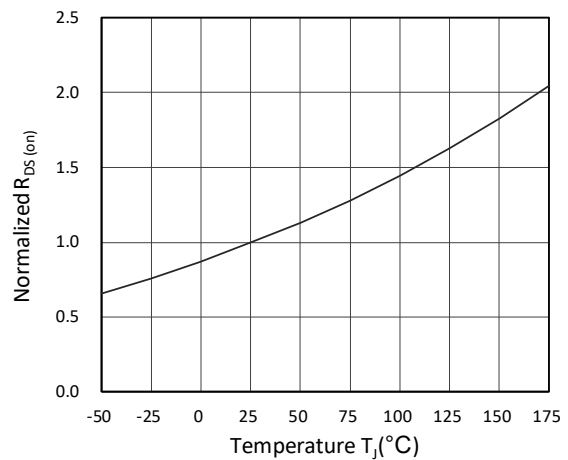


Figure 6. Normalized  $R_{DS(on)}$  vs. Temperature

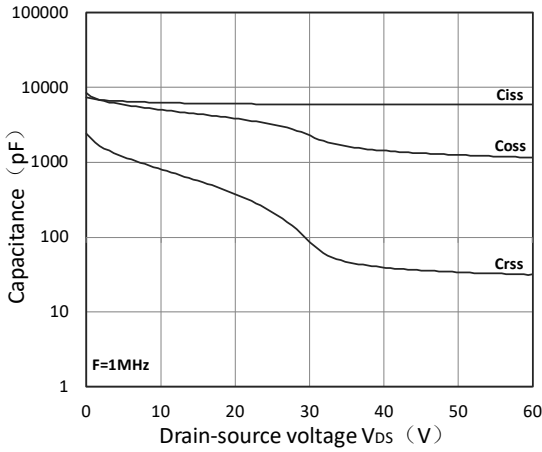


Figure 7. Capacitance Characteristics

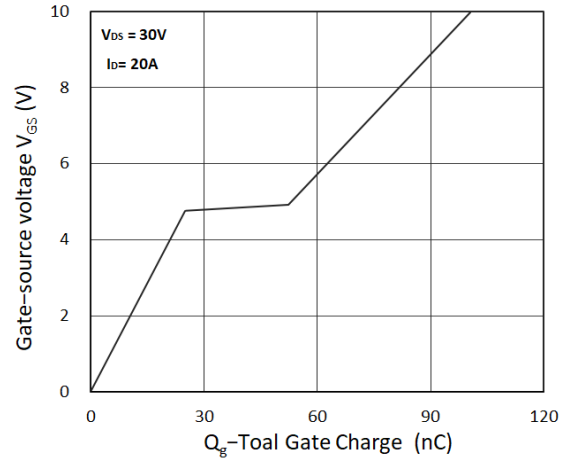


Figure 8. Gate Charge Characteristics

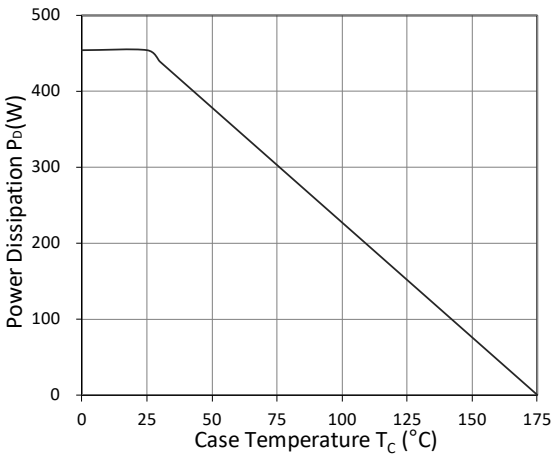


Figure 9. Power Dissipation

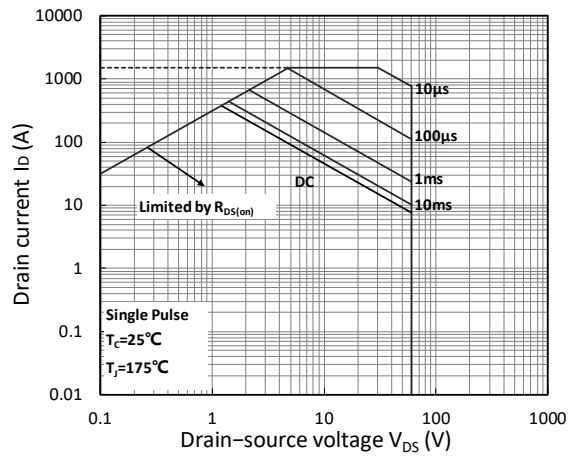


Figure 10. Safe Operating Area

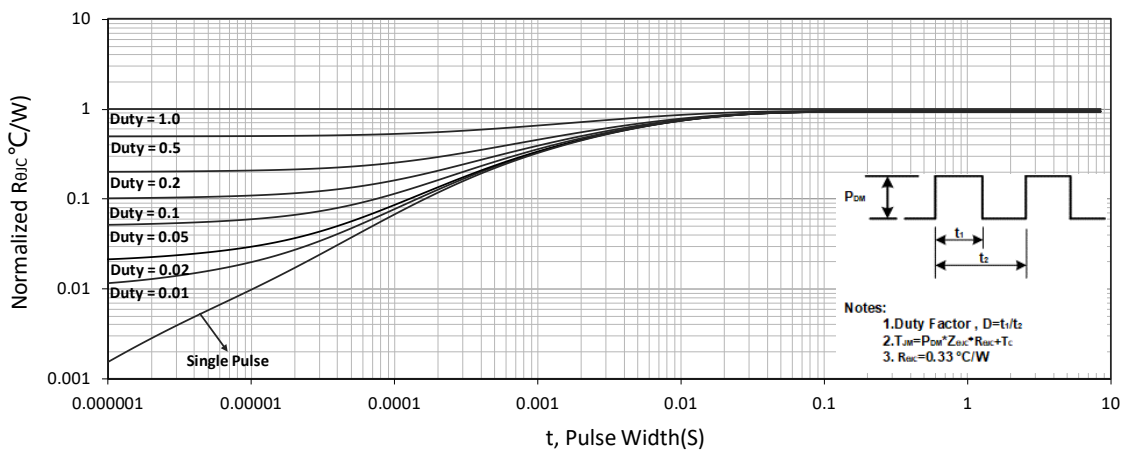


Figure 11. Normalized Maximum Transient Thermal Impedance



### Test Circuit

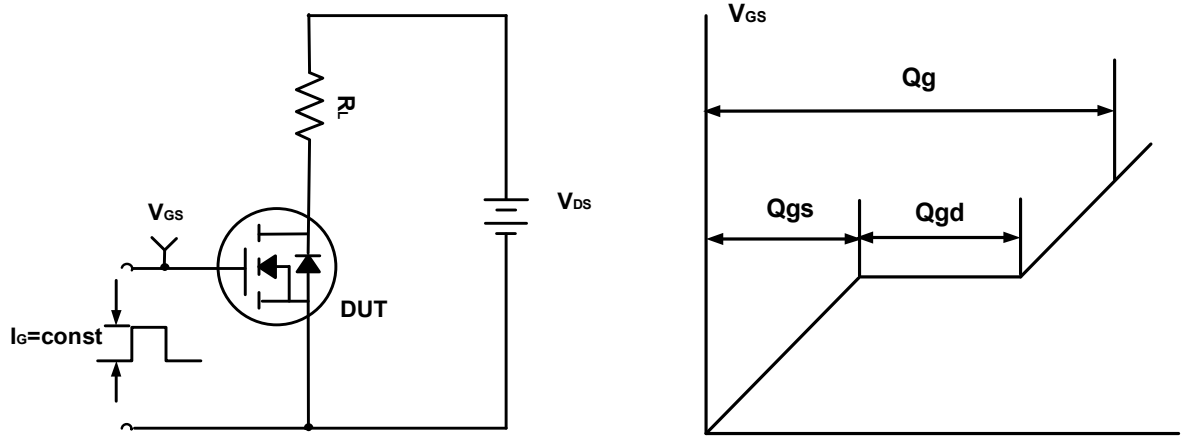


Figure A. Gate Charge Test Circuit & Waveforms

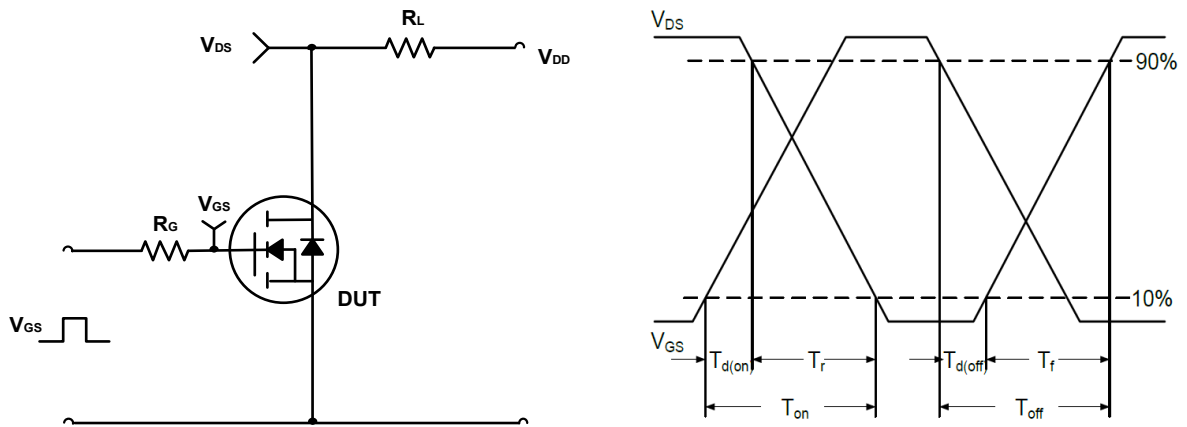


Figure B. Switching Test Circuit & Waveforms

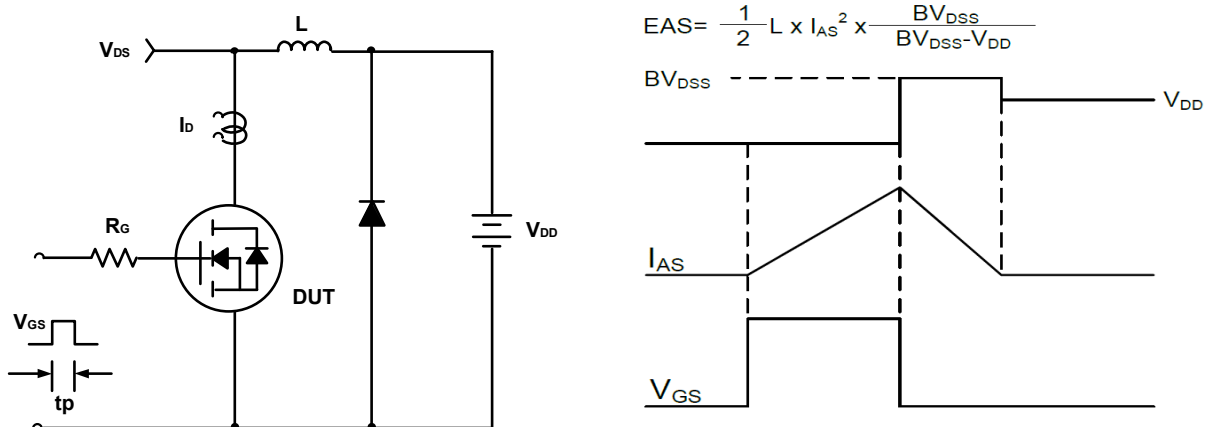
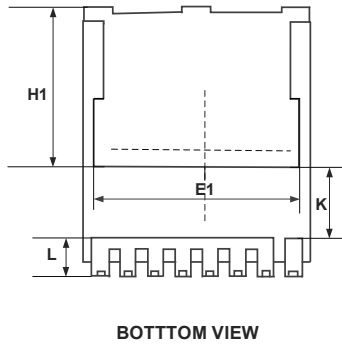
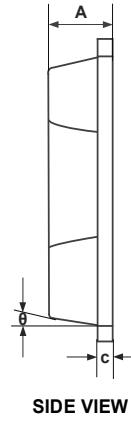
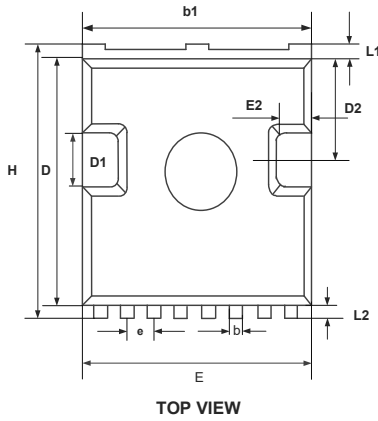


Figure C. Unclamped Inductive Switching Circuit & Waveforms



### Mechanical Dimensions for TOLL-8L



### COMMON DIMENSIONS

SYMBOL	MM	
	MIN	MAX
A	2.20	2.40
b	0.60	0.90
b1	9.70	9.90
c	0.40	0.60
D	10.20	10.60
D1	3.10	3.50
D2	4.45	4.75
E	9.70	10.10
E1	7.80BSC	
E2	0.50	0.70
e	1.200 BSC	
H	11.45	11.90
H1	6.75 BSC	
K	3.10 REF	
L	1.70	2.10
L1	0.60	0.80
L2	0.50	0.70
θ	10° REF	



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