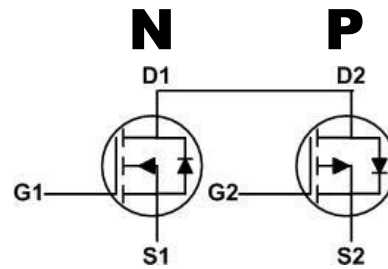




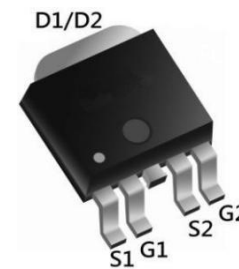
- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

### Description

The WLU3012 is the high performance complementary N-ch and P-ch MOSFETs with high cell density, which provide excellent R<sub>DS(on)</sub> and gate charge for most of the synchronous buck converter applications. The WLU3012 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.



### TO252-4 Pin Configuration



### Product Summary

BVDSS	R <sub>DS(on)</sub>	I <sub>D</sub>
30V	15 mΩ	12A
-30V	35 mΩ	-12A

### Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
V <sub>DS</sub>	Drain-Source Voltage	30	-30	V
V <sub>GS</sub>	Gate-Source Voltage	±20	±20	V
I <sub>D</sub> @T <sub>C</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	12	- 12	A
I <sub>D</sub> @T <sub>C</sub> =100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	10	- 8	A
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	30	-30	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	24.6	28	mJ
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation <sup>4</sup>	10.8	10.8	W
P <sub>D</sub> @T <sub>A</sub> =25°C	Total Power Dissipation <sup>4</sup>	2	2	W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	-55 to 150	°C
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	-55 to 150	°C

### Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R <sub>θJA</sub>	Thermal Resistance Junction-Ambient <sup>1</sup>	---	32	°C/W
R <sub>θJC</sub>	Thermal Resistance Junction-Case <sup>1</sup>	---	6	°C/W



**Electrical Characteristics** ( $T_J=25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=30V, V_{GS}=0V,$	-	-	1.0	$\mu A$
$I_{GSS}$	Gate to Body Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.5	2.5	V
$R_{DS(on)}$	Static Drain-Source on-Resistance <small>note3</small>	$V_{GS}=10V, I_D=5A$	-	15	20	m $\Omega$
		$V_{GS}=4.5V, I_D=3A$	-	21	29	
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS}=15V, V_{GS}=0V,$ $f=1.0MHz$	-	490	-	pF
$C_{oss}$	Output Capacitance		-	79	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	61	-	pF
$Q_g$	Total Gate Charge	$V_{DS}=15V, I_D=5.8A,$ $V_{GS}=10V$	-	10	-	nC
$Q_{gs}$	Gate-Source Charge		-	1.7	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge		-	2.5	-	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=15V, I_D=3A,$ $V_{GS}=10V, R_{REN}=3\Omega$	-	6	-	ns
$t_r$	Turn-on Rise Time		-	15	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	17	-	ns
$t_f$	Turn-off Fall Time		-	17	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain to Source Diode Forward Current		-	-	12	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	30	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS}=0V, I_S=9A$	-	-	1.2	V
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=5A, di/dt=100A/\mu s$	-	7	-	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge		-	2	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition :  $T_J=25^\circ\text{C}, V_{DD}=15V, V_G=10V, L=0.5mH, R_g=25\Omega, I_{AS}=6A$

3. Pulse Test: Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 0.5\%$



**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>Static Characteristics</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-30	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -30V, V <sub>GS</sub> = 0V	-	-	-1	μA
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
Gate-Source Threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	-1	-1.5	-2.5	V
Drain-Source on-State Resistance <sup>3</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -4.1A	-	35	50	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -3A	-	49	75	
<b>Dynamic Characteristics<sup>4</sup></b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V , V <sub>DS</sub> = -15V, f = 1.0MHz	-	530	-	pF
Output Capacitance	C <sub>oss</sub>		-	70	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	56	-	
<b>Switching Characteristics<sup>4</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = -10V, V <sub>DS</sub> = -15V, I <sub>D</sub> = -4.1A	-	6.8	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	1.0	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	1.4	-	
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = -10V, V <sub>DS</sub> = -15V , R <sub>L</sub> = 15Ω,R <sub>GEN</sub> = 2.5Ω	-	14	-	ns
Rise Time	t <sub>r</sub>		-	61	-	
Turn-off Delay time	t <sub>d(off)</sub>		-	19	-	
Fall Time	t <sub>f</sub>		-	10	-	
<b>Source-Drain Body Diode Characteristics</b>						
Diode Forward Voltage <sup>3</sup>	V <sub>SD</sub>	I <sub>S</sub> = -4.1A, V <sub>GS</sub> = 0V	-	-	-1.2	V
Continuous Source Current	I <sub>S</sub>		-	-	-12	A

**Notes:**

1. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C.
2. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
3. Pulse Test: Pulse width≤300μs, duty cycle≤2%.
4. This value is guaranteed by design hence it is not included in the production test.



N-Channel Typical Characteristics

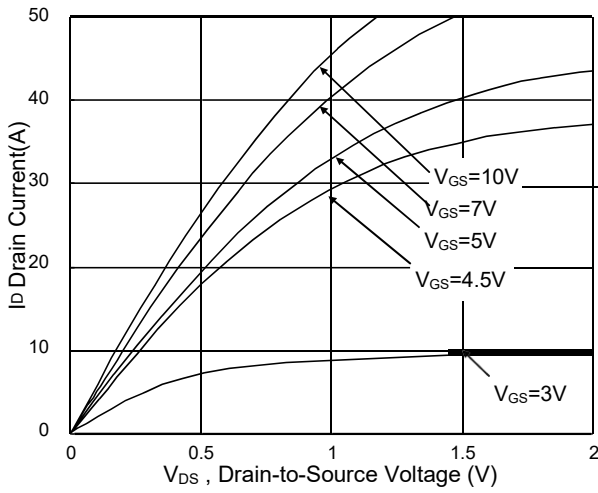


Fig.1 Typical Output Characteristics

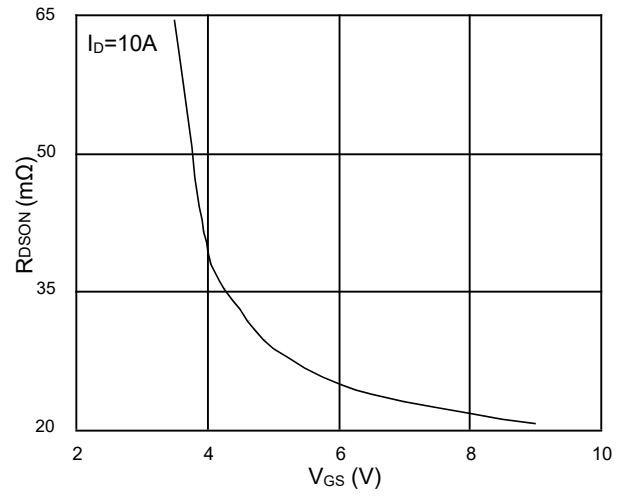


Fig.2 On-Resistance vs. Gate-Source

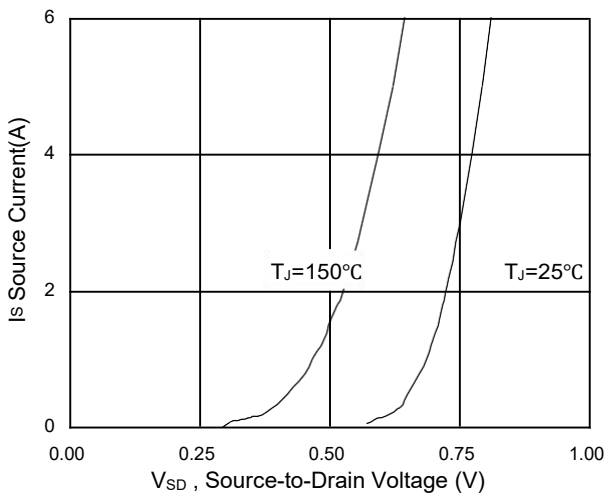


Fig.3 Forward Characteristics Of Reverse

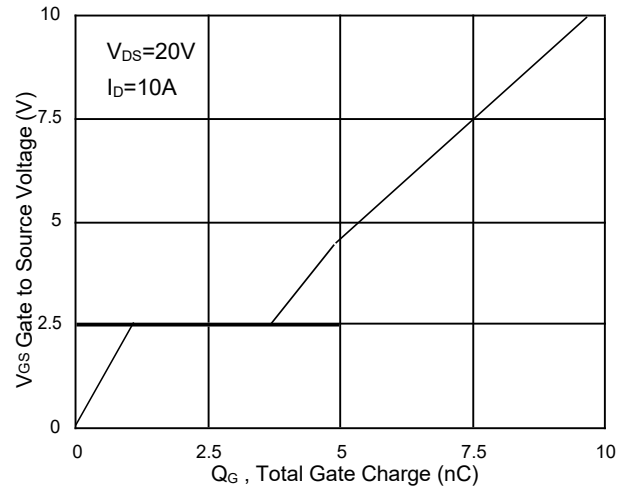


Fig.4 Gate-Charge Characteristics

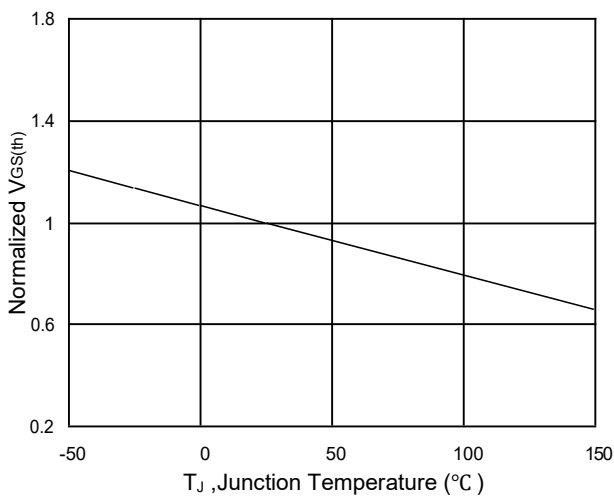


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$

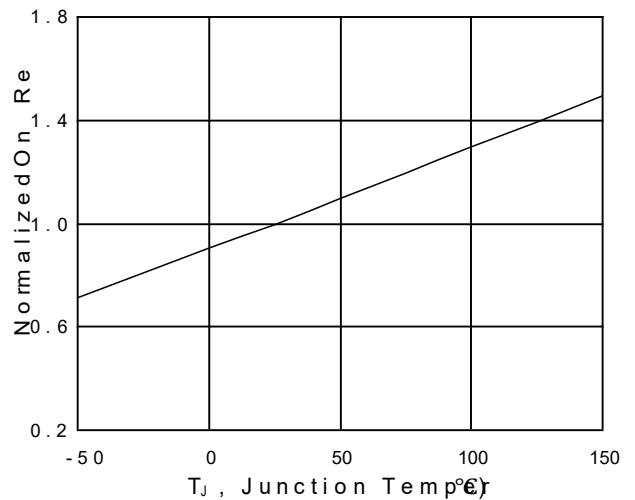


Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$

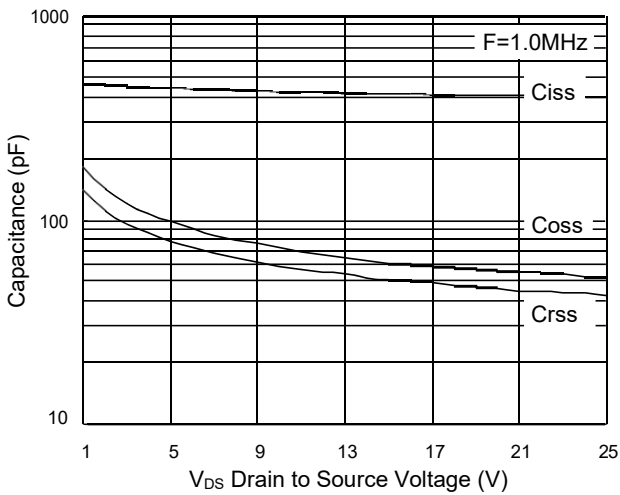


Fig.7 Capacitance

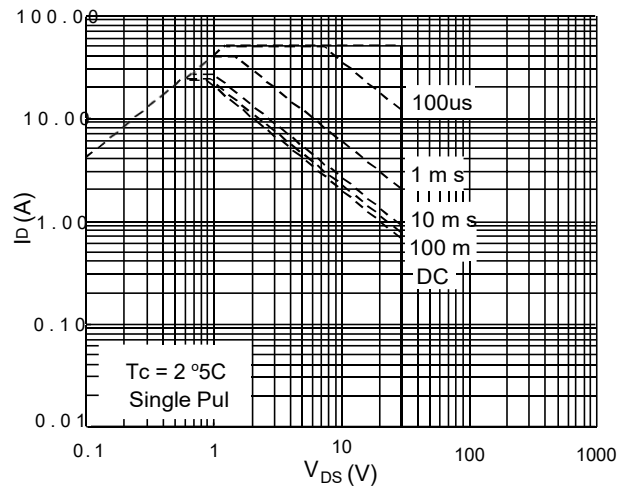


Fig.8 Safe Operating Area

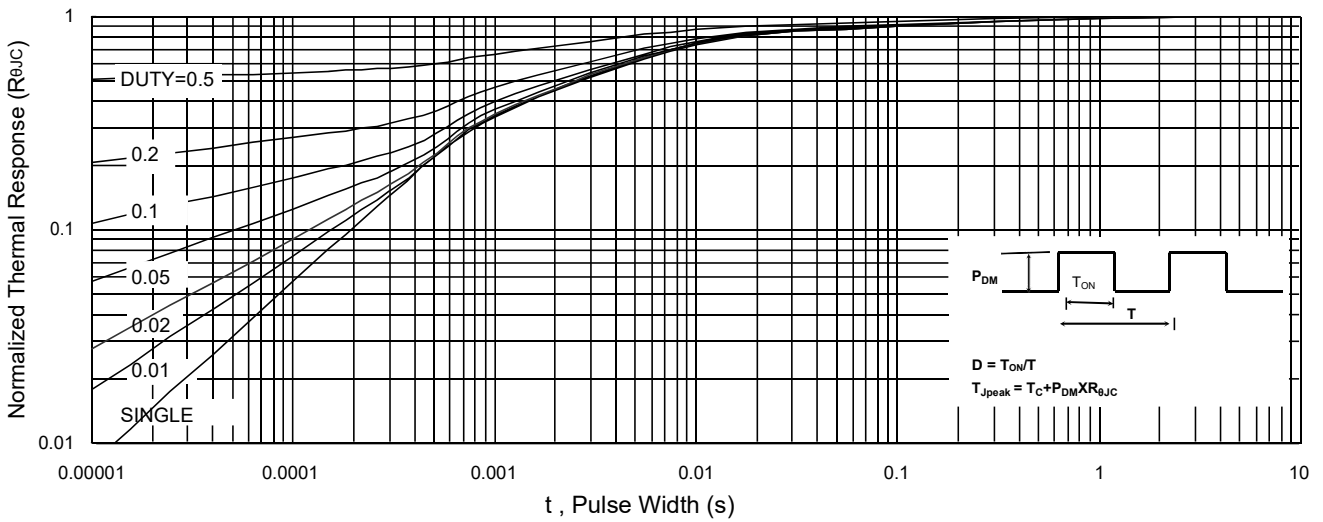
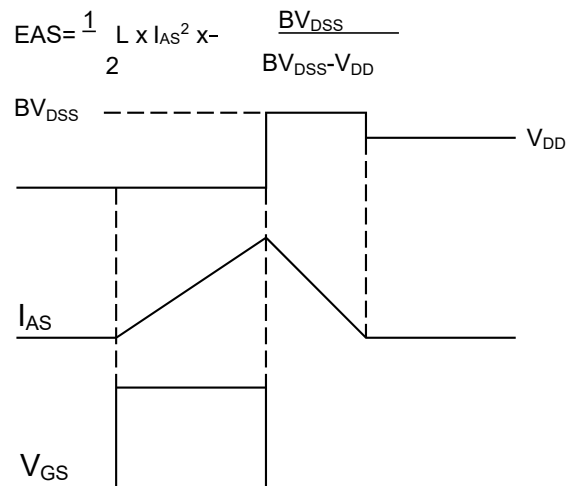
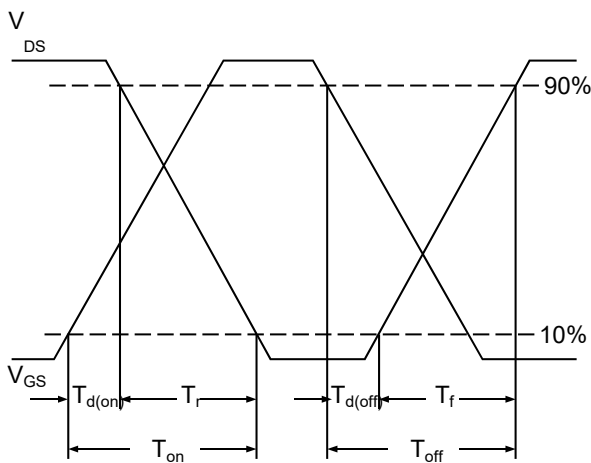


Fig.9 Normalized Maximum Transient Thermal Impedance





P-Channel Typical Characteristics

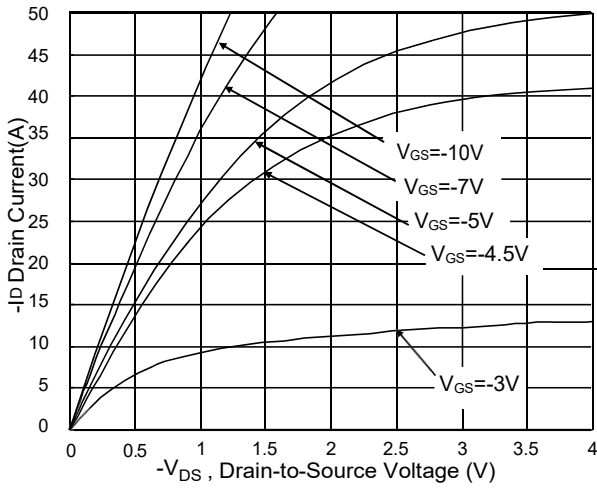


Fig.1 Typical Output Characteristics

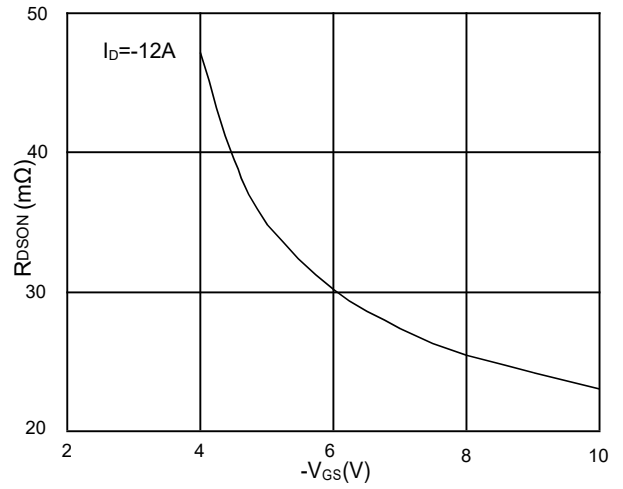


Fig.2 On-Resistance v.s Gate-Source

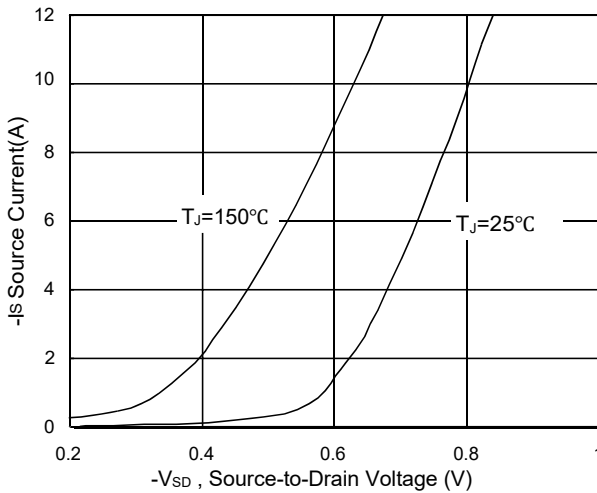


Fig.3 Forward Characteristics Of Reverse

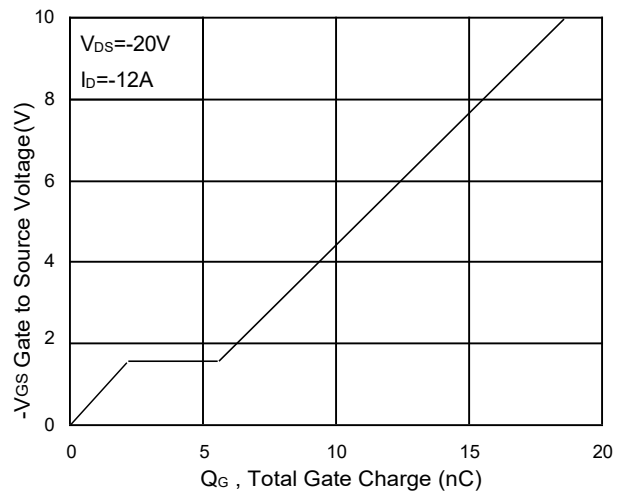


Fig.4 Gate-Charge Characteristics

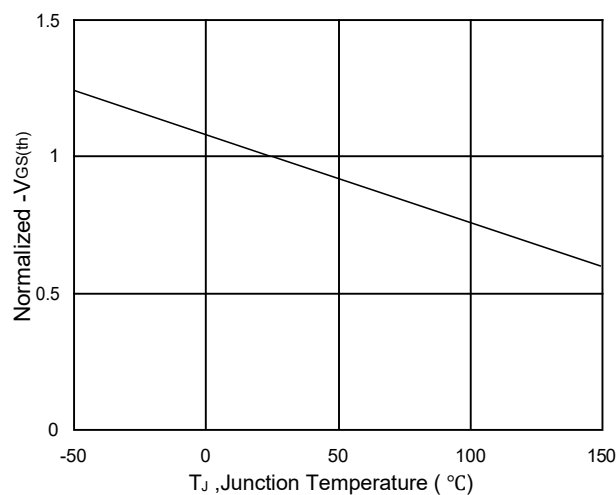


Fig.5 Normalized VGS(th) v.s TJ

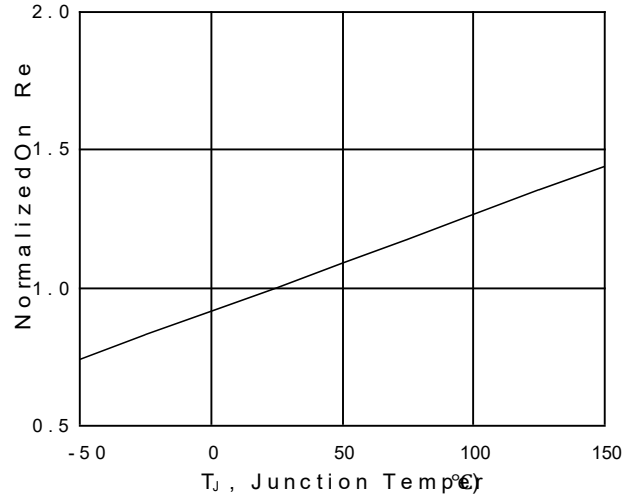


Fig.6 Normalized RDS(on) v.s TJ

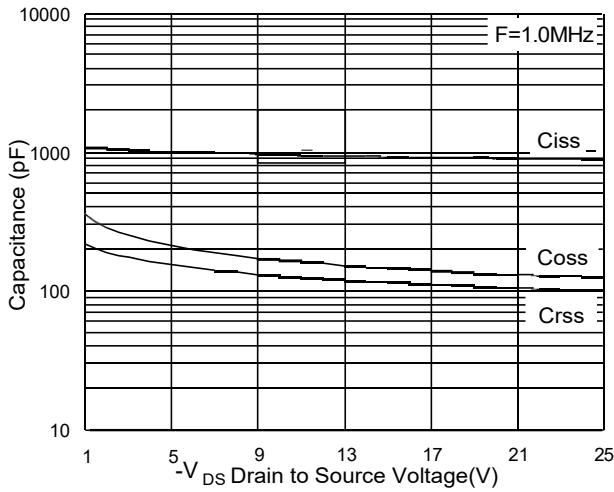


Fig.7 Capacitance

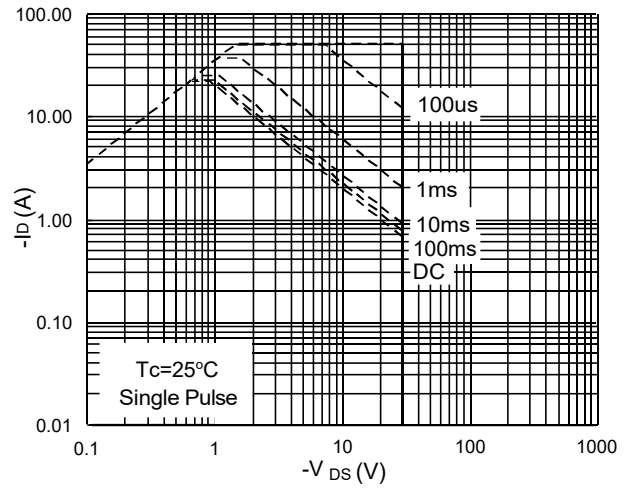


Fig.8 Safe Operating Area

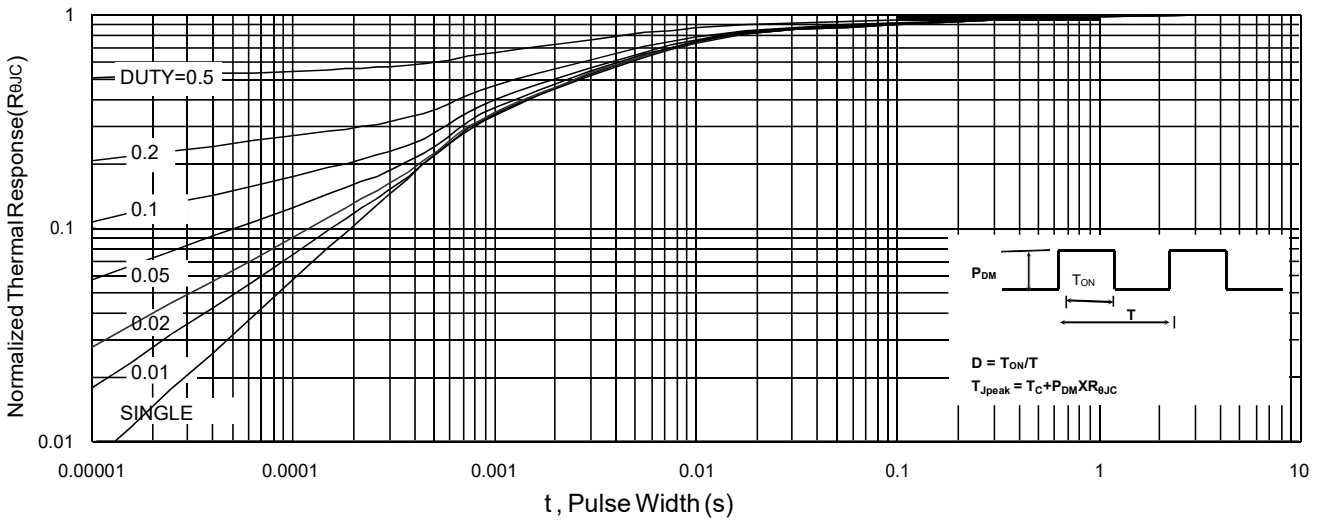


Fig.9 Normalized Maximum Transient Thermal Impedance

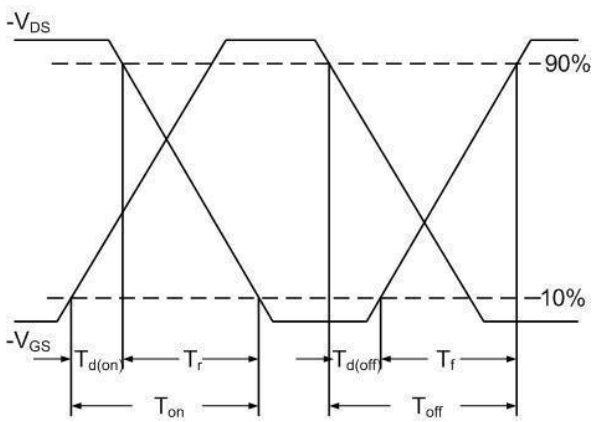


Fig.10 Switching Time Waveform

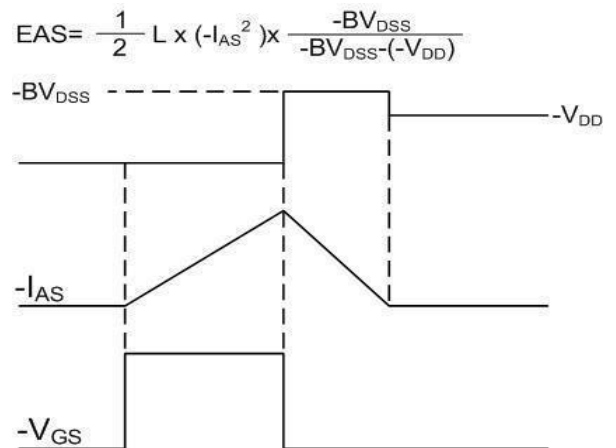
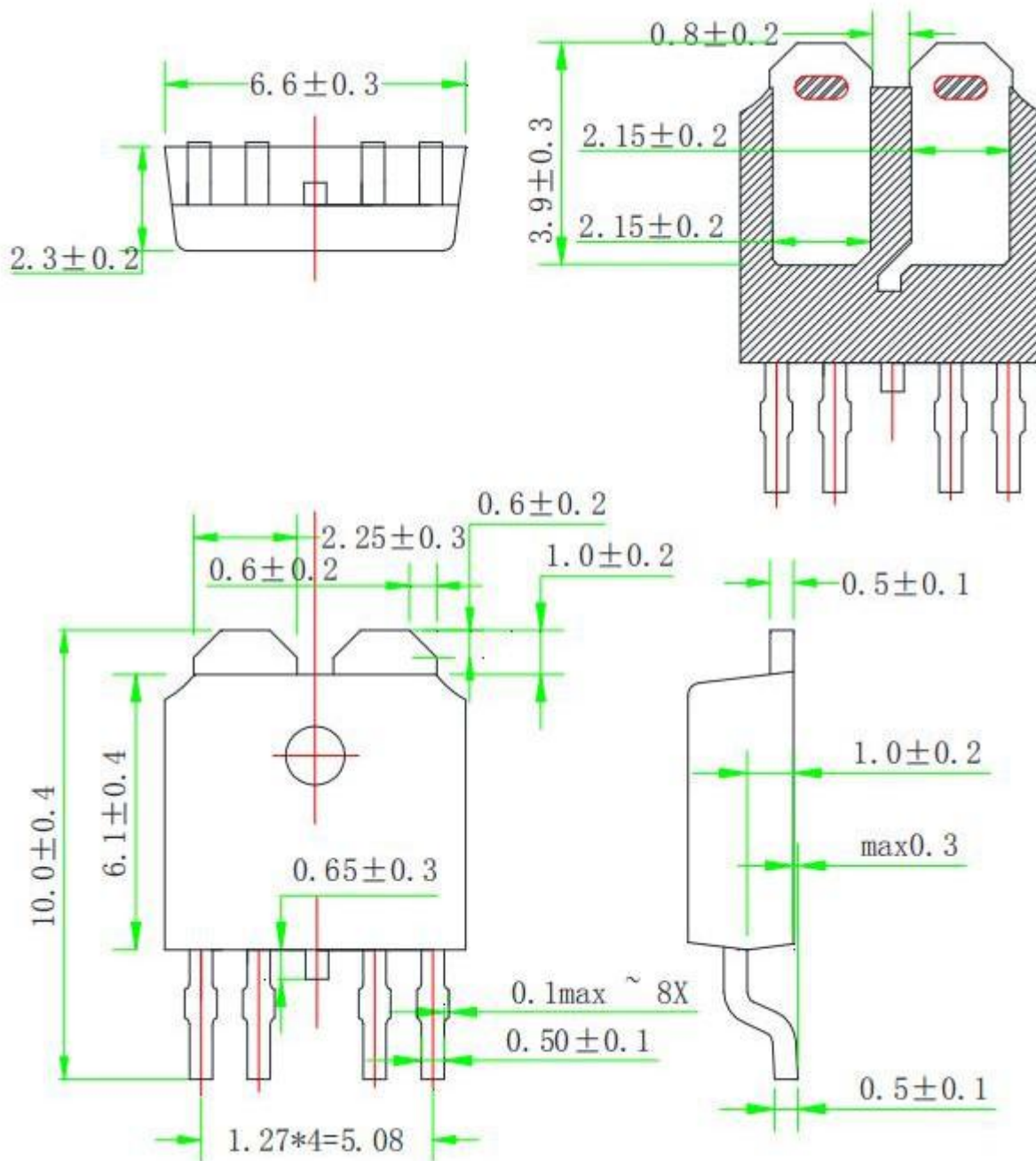


Fig.11 Unclamped Inductive Switching Waveform





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